

Fauchon 13" Intel Broadwell-U UMA Schematic

Broadwell-U 15W

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REV:SA

2014-08-13

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Title

Cover Page

Size
A4

Document Number

Fauchon-BDW 13"

Rev

SA

Date: Saturday, September 13, 2014

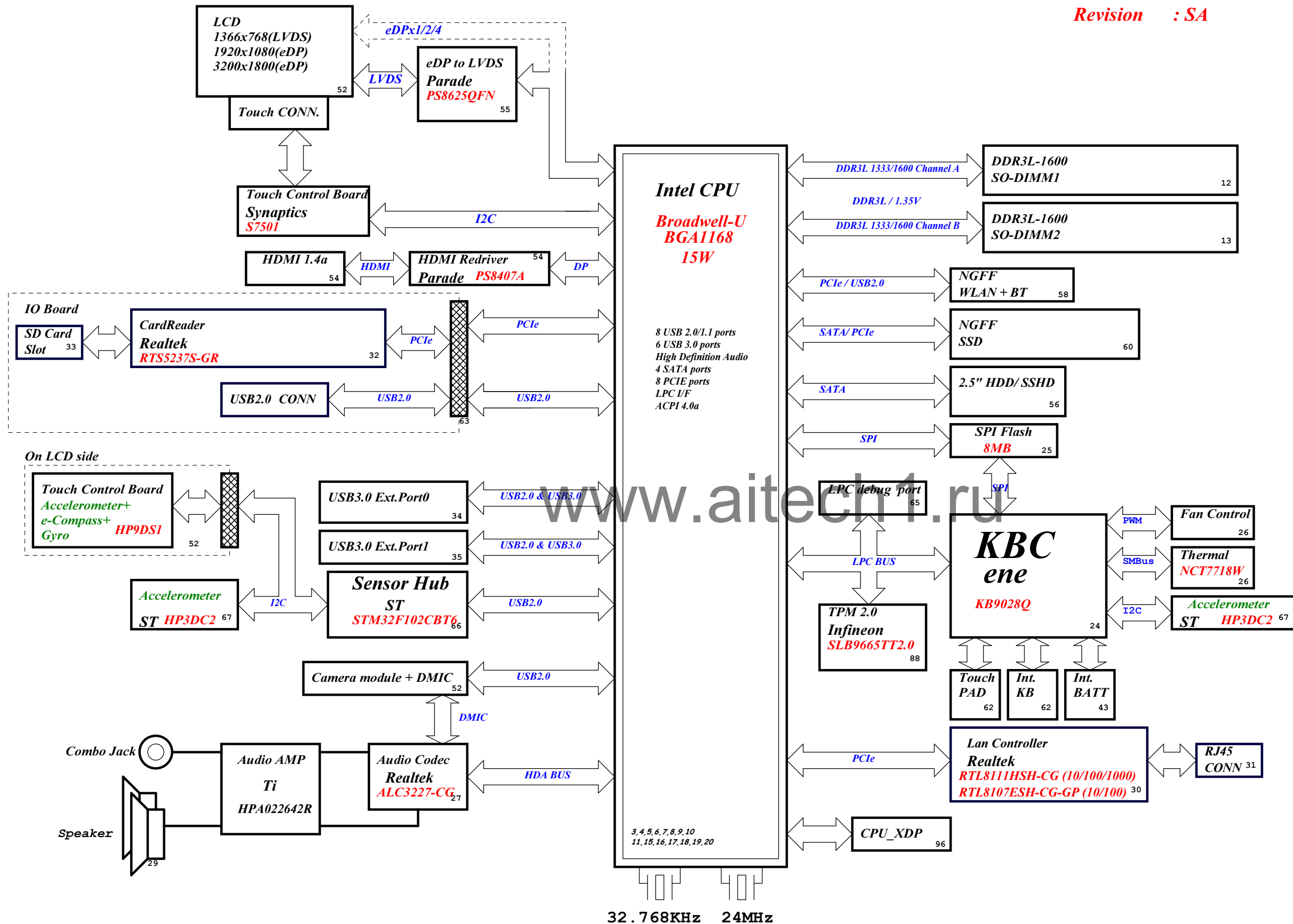
Sheet 1 of 102

Fauchon 13" Block Diagram

Project code : 4PD045010001

PCB P/N : 14259

Revision : SA



CHARGER	
HPA02224RGRR 44	
INPUTS	OUTPUTS
AD+ BT+	DCBATOUT
SYSTEM DC/DC	
TPS51225RUKR-GP 45	
INPUTS	OUTPUTS
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5 5V_S5 3D3V_S5
CPU DC/DC	
TPS51624RSMR 46,47	
INPUTS	OUTPUTS
DCBATOUT	CPU_CORE
SYSTEM DC/DC	
RT8068AZQWID 51	
INPUTS	OUTPUTS
DCBATOUT	1D5V_S0
SYSTEM DC/DC	
SY8208DQNC 48	
INPUTS	OUTPUTS
DCBATOUT	1D05V_LAN
SYSTEM DC/DC	
TPS51716RUKR 49	
INPUTS	OUTPUTS
DCBATOUT	1D35V_PWR
VGA	
RT8179CGQW 80,81	
INPUTS	OUTPUTS
DCBATOUT	VGA_CORE
VGA	
RT8068AZQWID SY8208DQNC 82	
INPUTS	OUTPUTS
3D3V_S5 DCBATOUT	1D8V 0D95V
PCB LAYER	
L1: TOP L2: GND L3: Signal L4: Signal L5: GND/PWR L6: BOTTOM	

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Block Diagram	
Size	Document Number
Custom	Fauchon-BDW 13"
Date: Thursday, September 18, 2014	Rev SA
Sheet 2	of 102

SSID = CPU

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Title

CPU (Reserved)

Size
A4

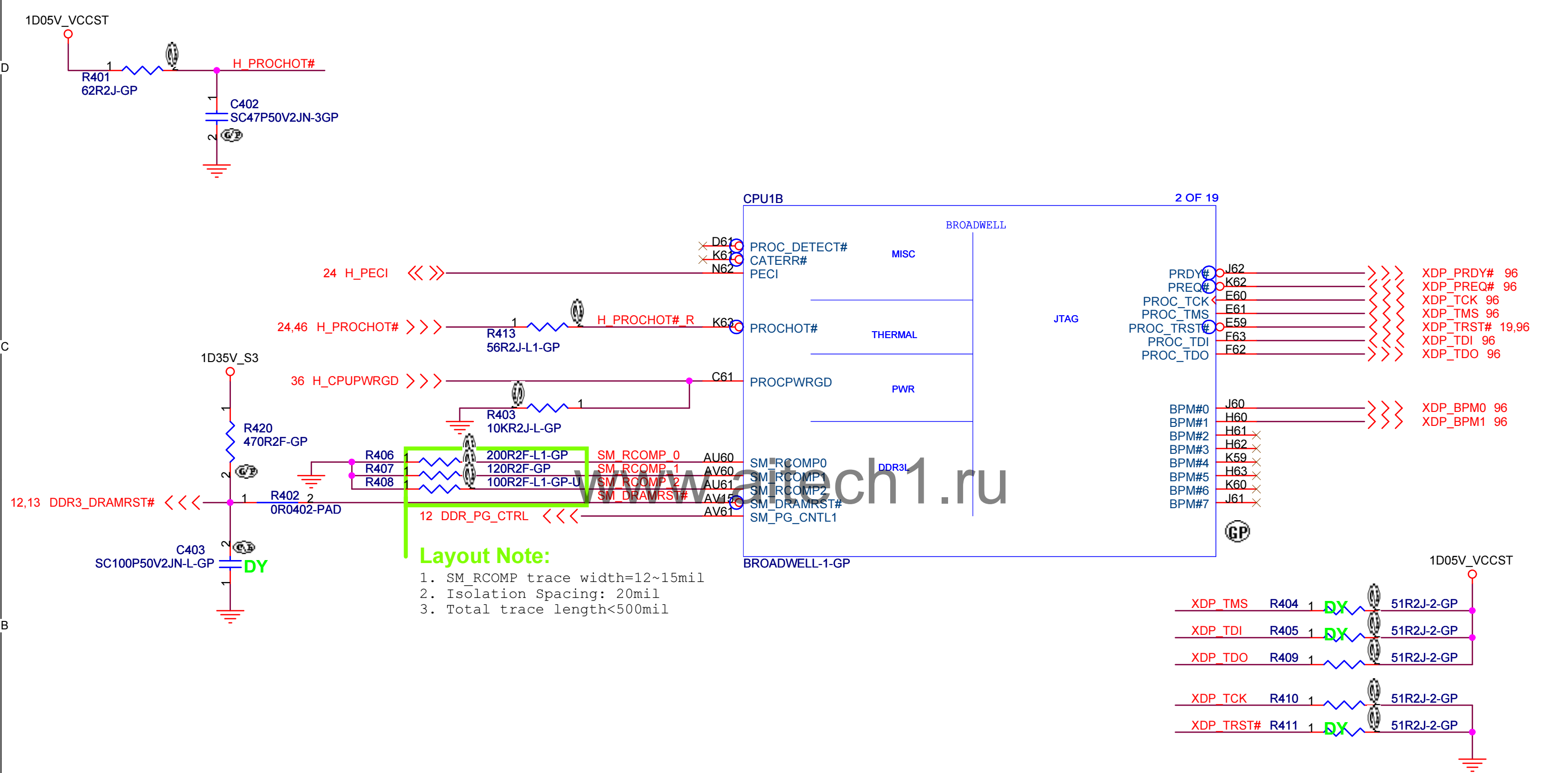
Document Number
Fauchon-BDW 13"

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Rev
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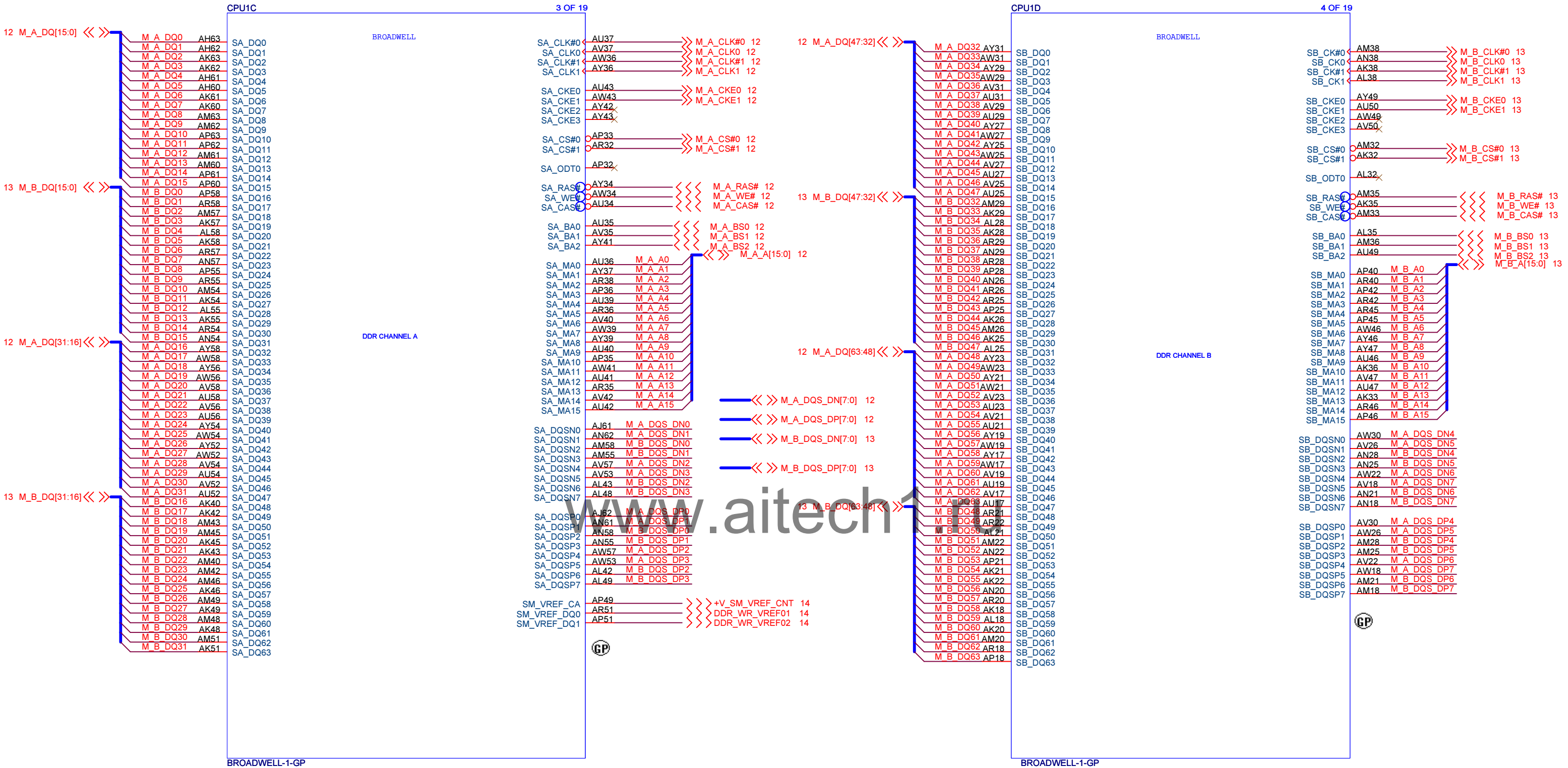
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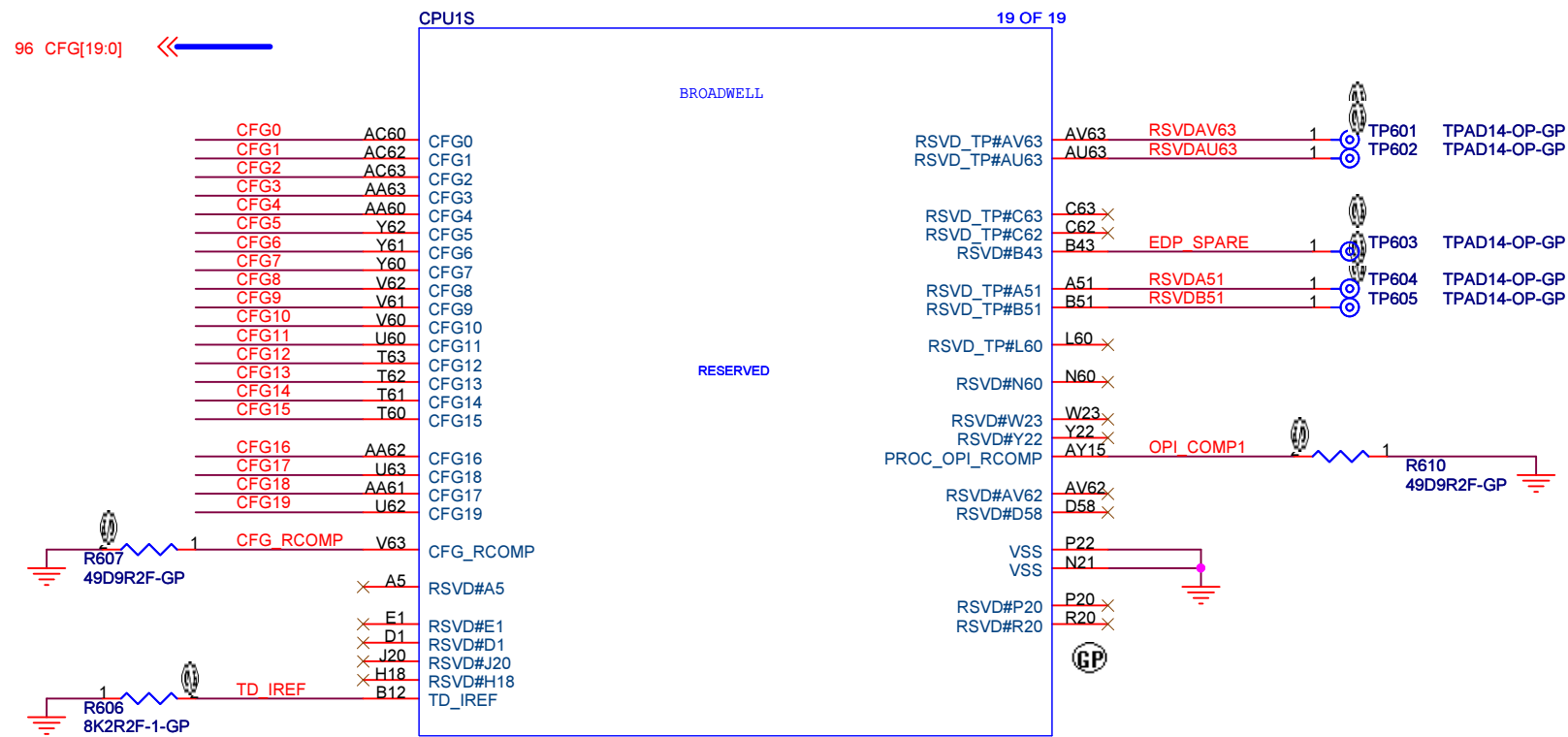


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Title CPU (DDR)
Size A3 Document Number Fauchon-BDW 13"
Date: Monday, October 27, 2014 Sheet 5 of 102 Rev SA

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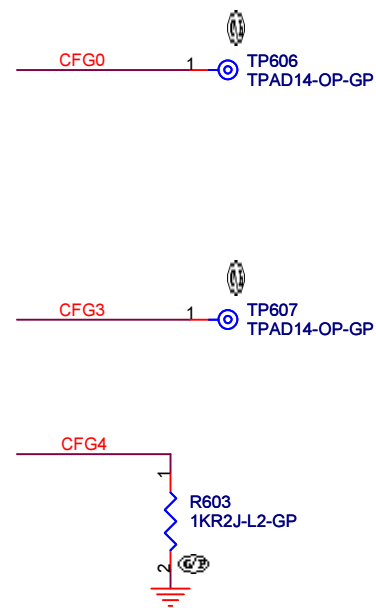


7.4

Reserved or Unused Signals

The following are the general types of reserved (RSVD) signals and connection guidelines:

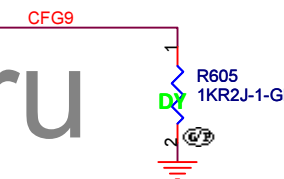
- RSVD – these signals should not be connected
- RSVD_TP – these signals should be routed to a test point
- RSVD_NCTF – these signals are non-critical to function and may be left unconnected



Pin Name	Strap Description	Configuration ¹ (Default value for each bit is 1 unless specified)	Default Value	✓
CFG[0]		Connect a series 1 kΩ resistor on the critical CFG[0] trace in a manner which does not introduce any stubs to CFG[0] trace. Route as needed from the opposite side of this series isolation resistor to the debug port. ITP will drive the net to GND.		

PHYSICAL_DEBUG_ENABLED (DFX PRIVACY)	
CFG[3]	0 : ENABLED SET DFX ENABLED BIT IN DEBUG INTERFACE MSR 1 : DISABLED

DISPLAY PORT PRESENCE STRAP	
CFG[4]	0 : ENABLED AN EXTERNAL DISPLAY PORT DEVICE IS CONNECTED TO THE EMBEDDED DISPLAY PORT 1 : DISABLED NO PHYSICAL DISPLAY PORT ATTACHED TO EMBEDDED DISPLAY PORT

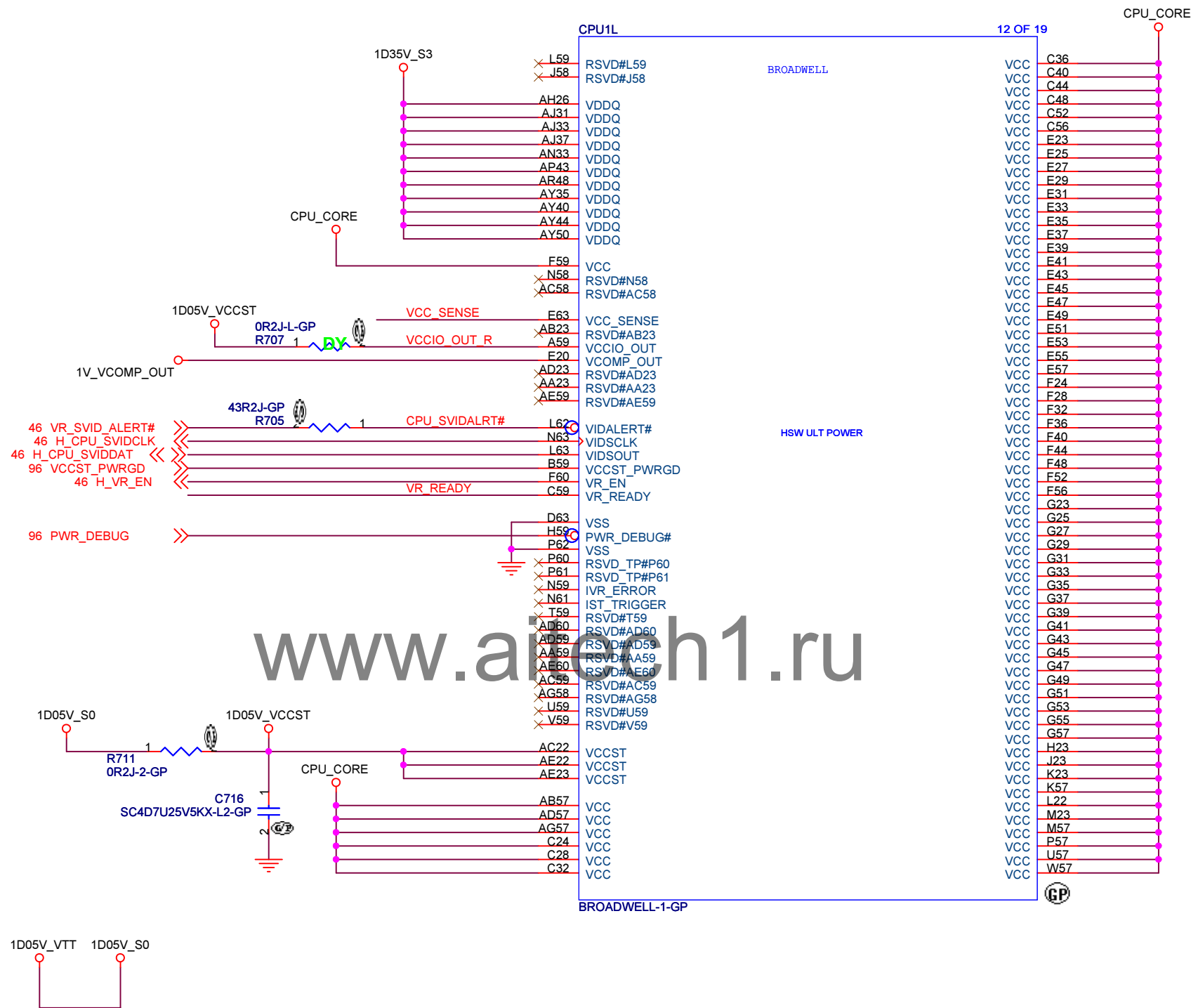
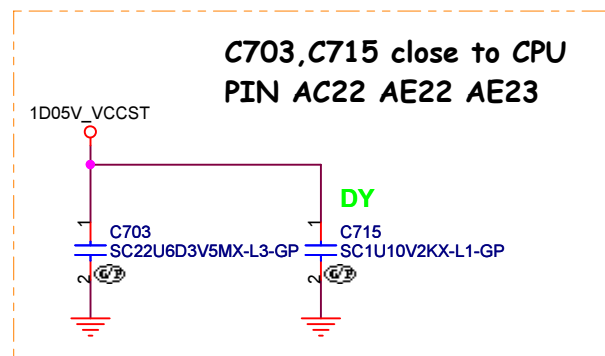
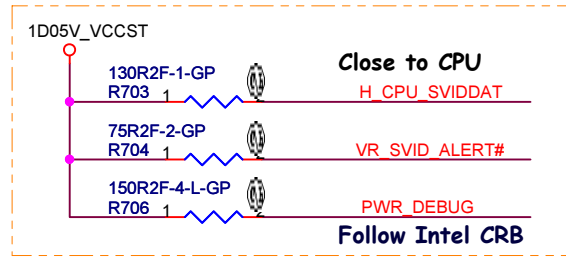


NO SVID PROTOCOL CAPABLE VR CONNECTED
0:NO VR SUPPORTING SVID IS PRESENT. THE CHIP WILL NOTGENERATE (OR RESPOND TO) SVID ACTIVITY
1:VRS SUPPORTING SVID PROTOCOL ARE PRESENT

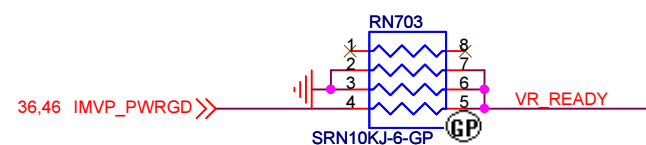
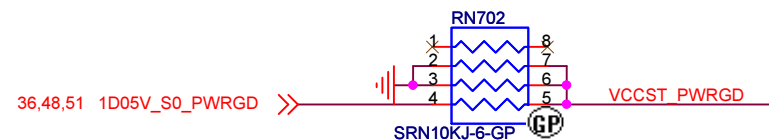
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Size Custom	Document Number Fauchon-BDW 13"
Date: Monday, October 27, 2014	Rev SA

SSID = CPU



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CPU (VCC_CORE)

Size
A3

Document Number

Fauchon-BDW 13"

Rev
SA

Date: Wednesday, October 29, 2014

Sheet

7

of

102

SSID = CPU

HDMI

54 HDMI_DATA_CPU_N2
54 HDMI_DATA_CPU_P2
54 HDMI_DATA_CPU_N1
54 HDMI_DATA_CPU_P1
54 HDMI_DATA_CPU_N0
54 HDMI_DATA_CPU_P0
54 HDMI_DATA_CPU_N3
54 HDMI_DATA_CPU_P3



C54 DD11_TXN0
C55 DD11_TXP0
B58 DD11_TXN1
C58 DD11_TXP1
B55 DD11_TXN2
A55 DD11_TXP2
A57 DD11_TXN3
B57 DD11_TXP3

C51 DD12_TXN0
C50 DD12_TXP0
C53 DD12_TXN1
B54 DD12_TXP1
C49 DD12_TXN2
B50 DD12_TXP2
A53 DD12_TXN3
B53 DD12_TXP3

CPU1A

BROADWELL

1 OF 19

EDP_TXN0
EDP_TXP0
EDP_TXN1
EDP_TXP1

EDP_TXN2
EDP_TXP2
EDP_TXN3
EDP_TXP3

EDP_AUXN
EDP_AUXP

EDP_RCOMP
EDP_DISP_UTIL

C45
B46
A47
B47

C47
C46
A49
B49

A45
B45

D20
A43

eDP_TX_CPU_N0 52,55
eDP_TX_CPU_P0 52,55
eDP_TX_CPU_N1 52,55
eDP_TX_CPU_P1 52,55

eDP

eDP_AUX_CPU_N 52,55
eDP_AUX_CPU_P 52,55

EDP_RCOMP 24D9R2F-L-GP

1V_VCOMP_OUT

R801



Layout Note:

Design Guideline:
EDP_COMP keep routing length max 100 mils.
Trace Width:20 mils.

Signal	Trace Width	Isolation Spacing	Resistor Value	Length
eDP_RCOMP	20 mils	25 mils	24.9 Ω \pm 1%	Max = 100 mils

Bit Rate	Supports (in # of lanes)	Peak Bandwidth
1.62 Gb/s	4	4 x 162 MB/s = 648 MB/s
5.4 Gb/s	4	4 x 540 MB/s = 2160 MB/s
2.7 Gb/s	4	4 x 270 MB/s = 1080 MB/s

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CPU (DDI/EDP)

Size A4

Document Number

Fauchon-BDW 13"

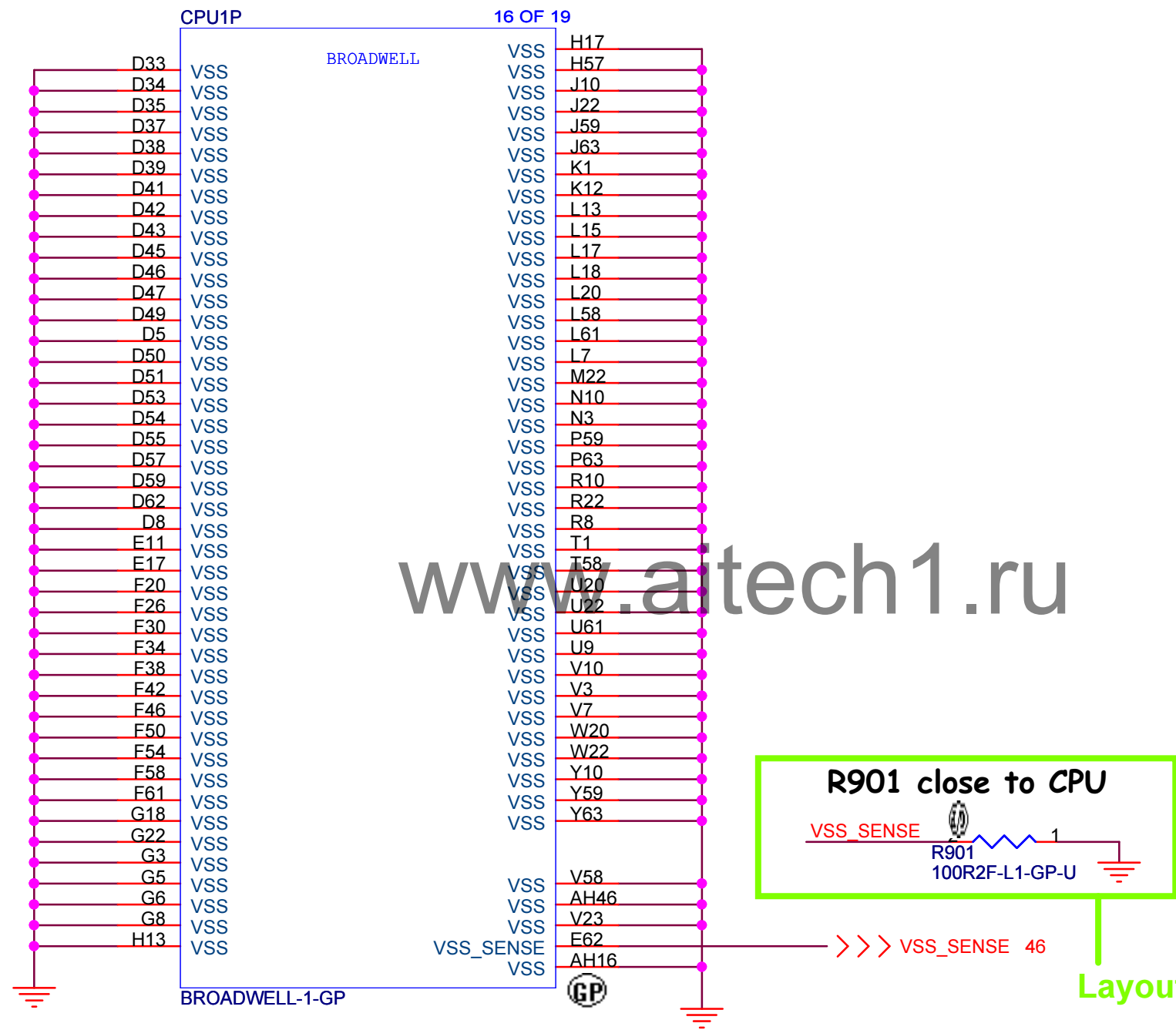
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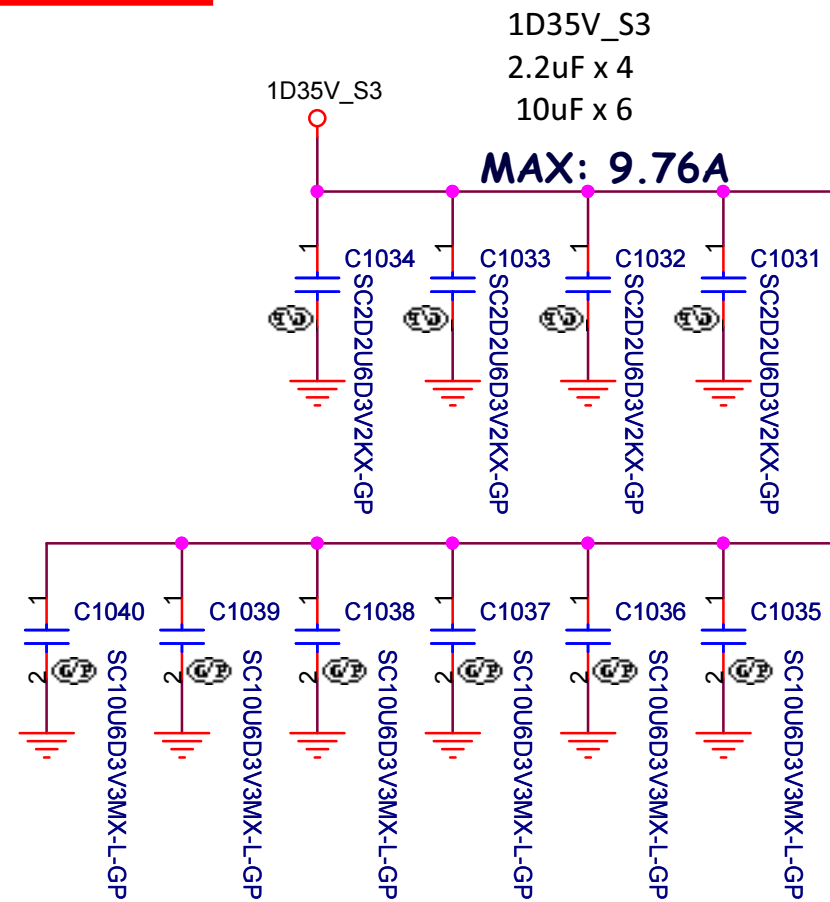
Sheet 8 of 102

SSID = CPU

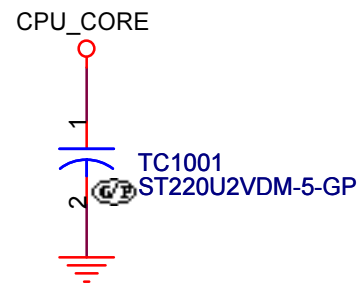
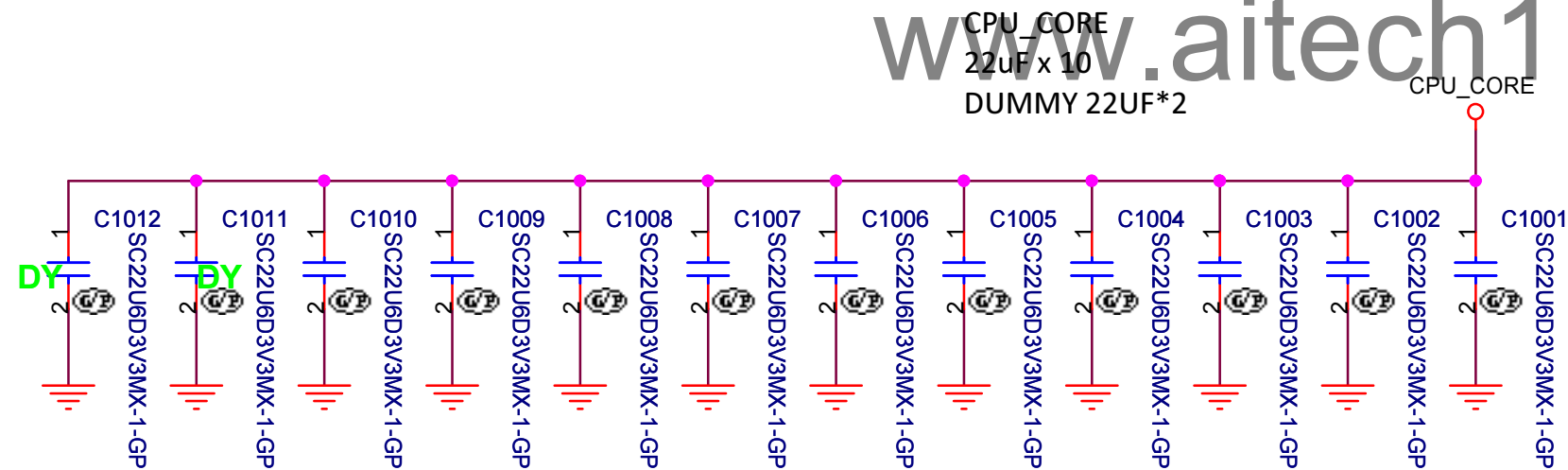


Layout Note:

SSID = MCP



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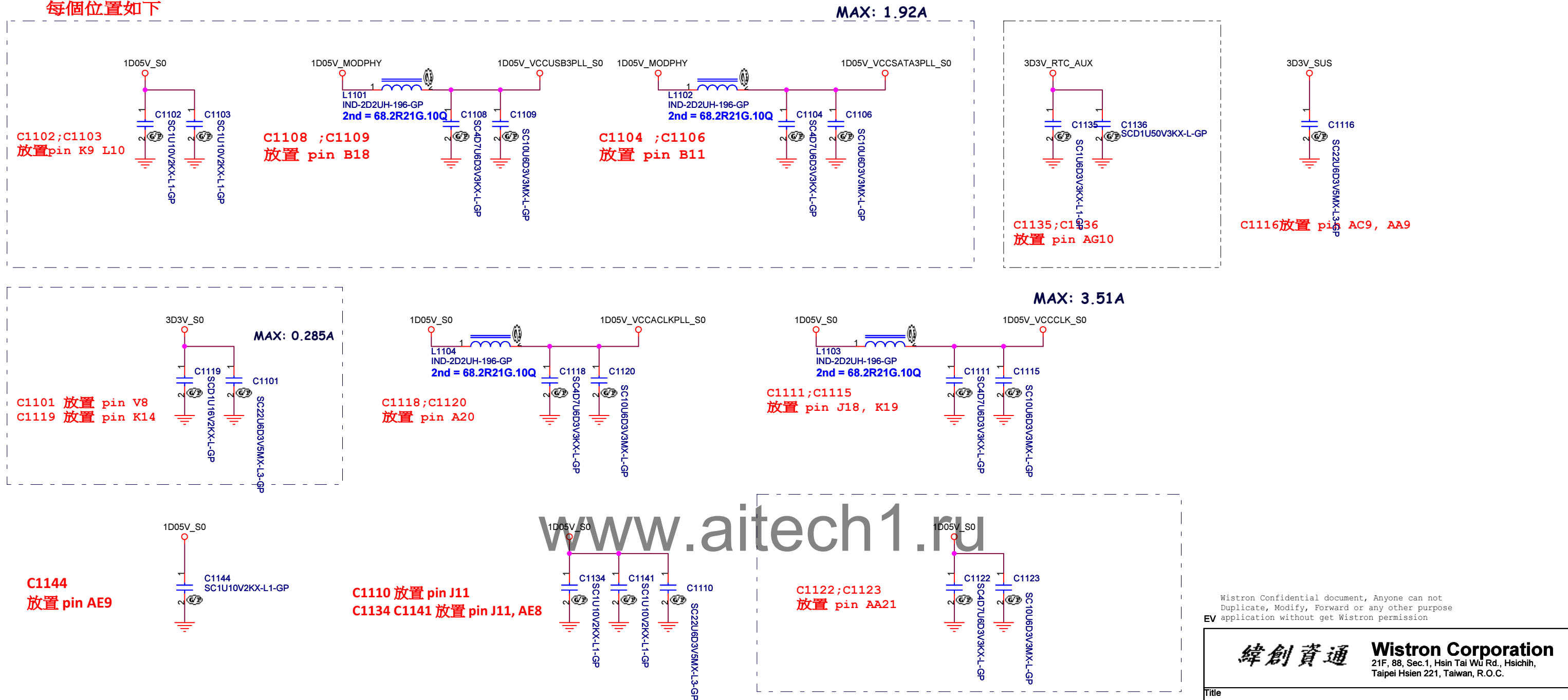
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Title		
CPU (Power CAP1)		
Size A4	Document Number Fauchon-BDW 13"	Rev SA
Date: Wednesday, October 15, 2014	Sheet 10 of	102

擺放電容的位置請參考Page 21
每個位置如下

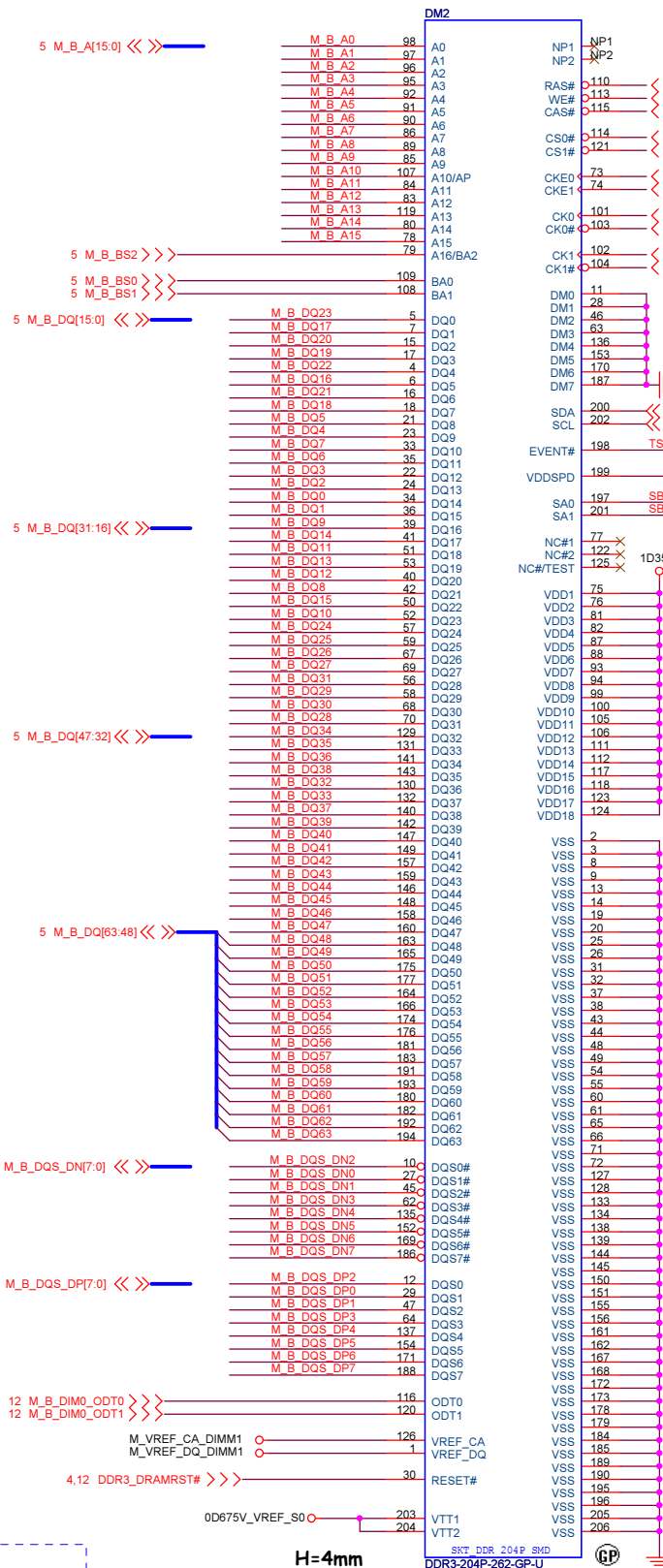


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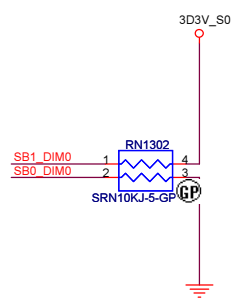
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Title	
CPU (Power CAP2)	
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Date:	Thursday, October 23, 2014
Sheet	11 of 102
Rev	
SA	

SSID = MEMORY

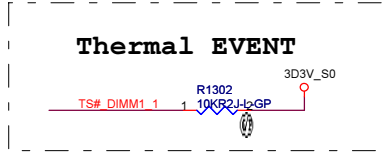


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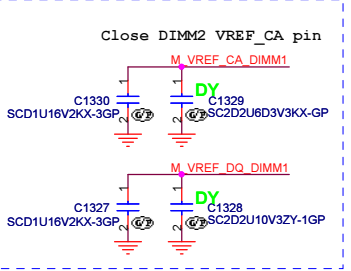
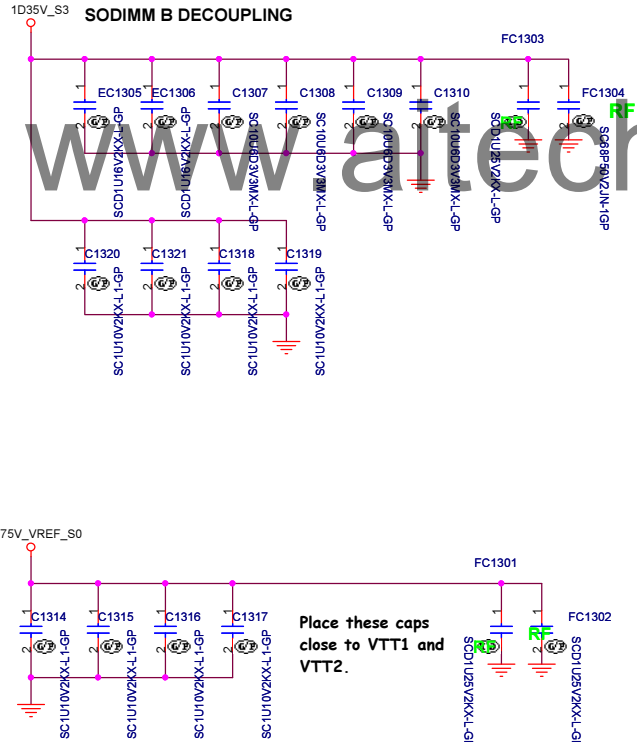


Note:
SO-DIMMB SPD Address is 0xA4
SO-DIMMB TS Address is 0x34

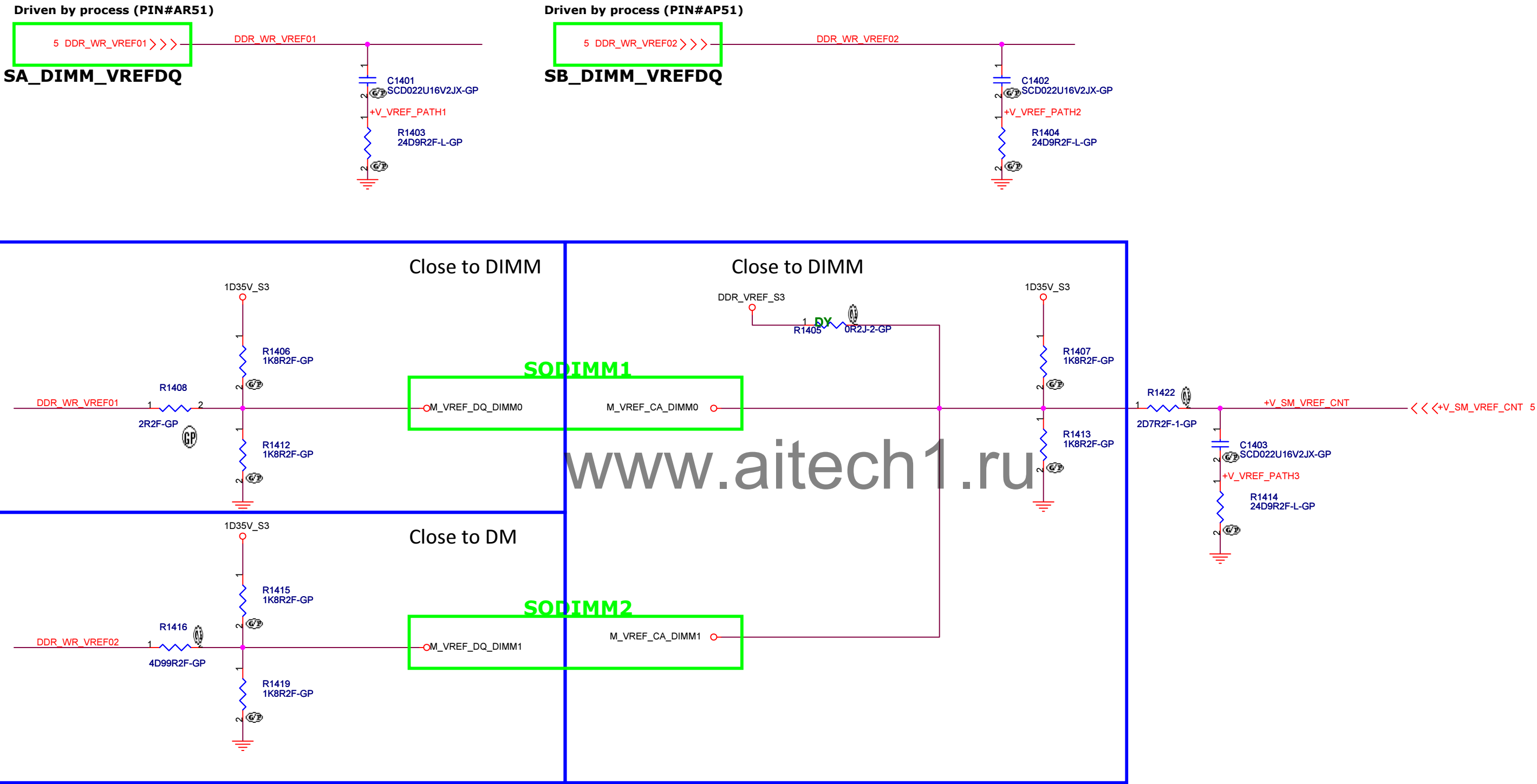
SO-DIMMB is placed farther from
the Processor than SO-DIMMA



Layout Note:
Place these Caps near
SO-DIMMB.



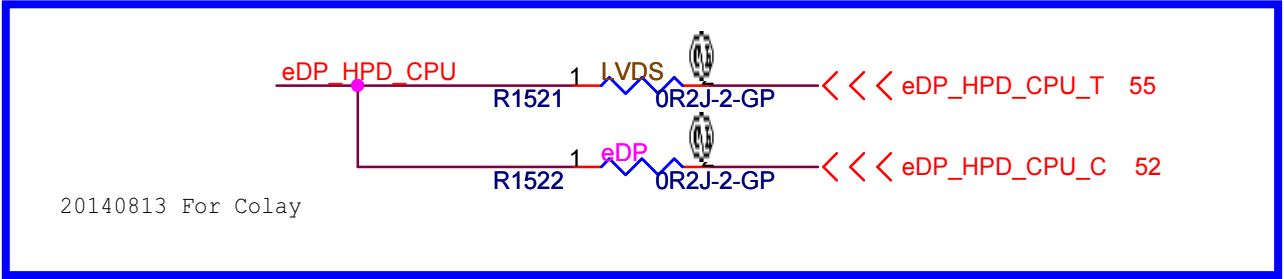
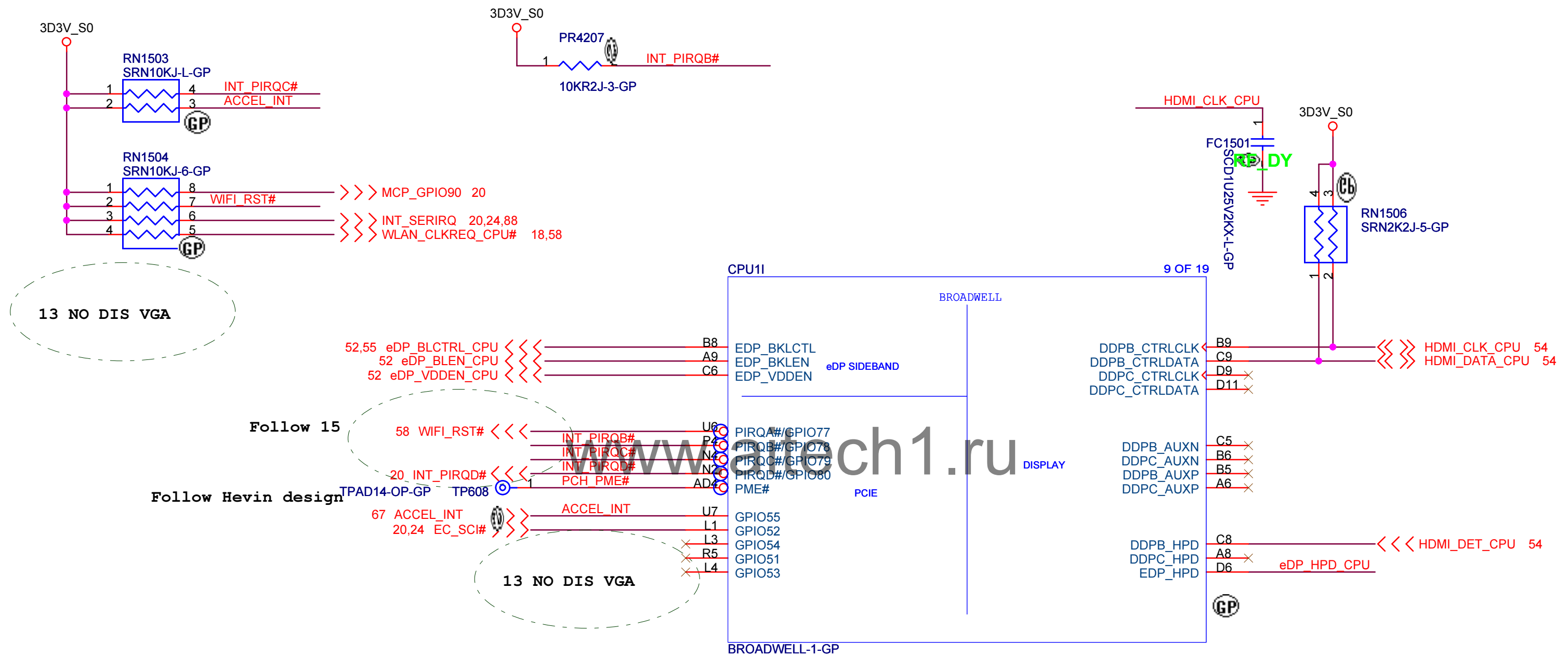
VREF circuit -M1 (Voltage Driver Network) & M3 (Driven by Processor) Implementation



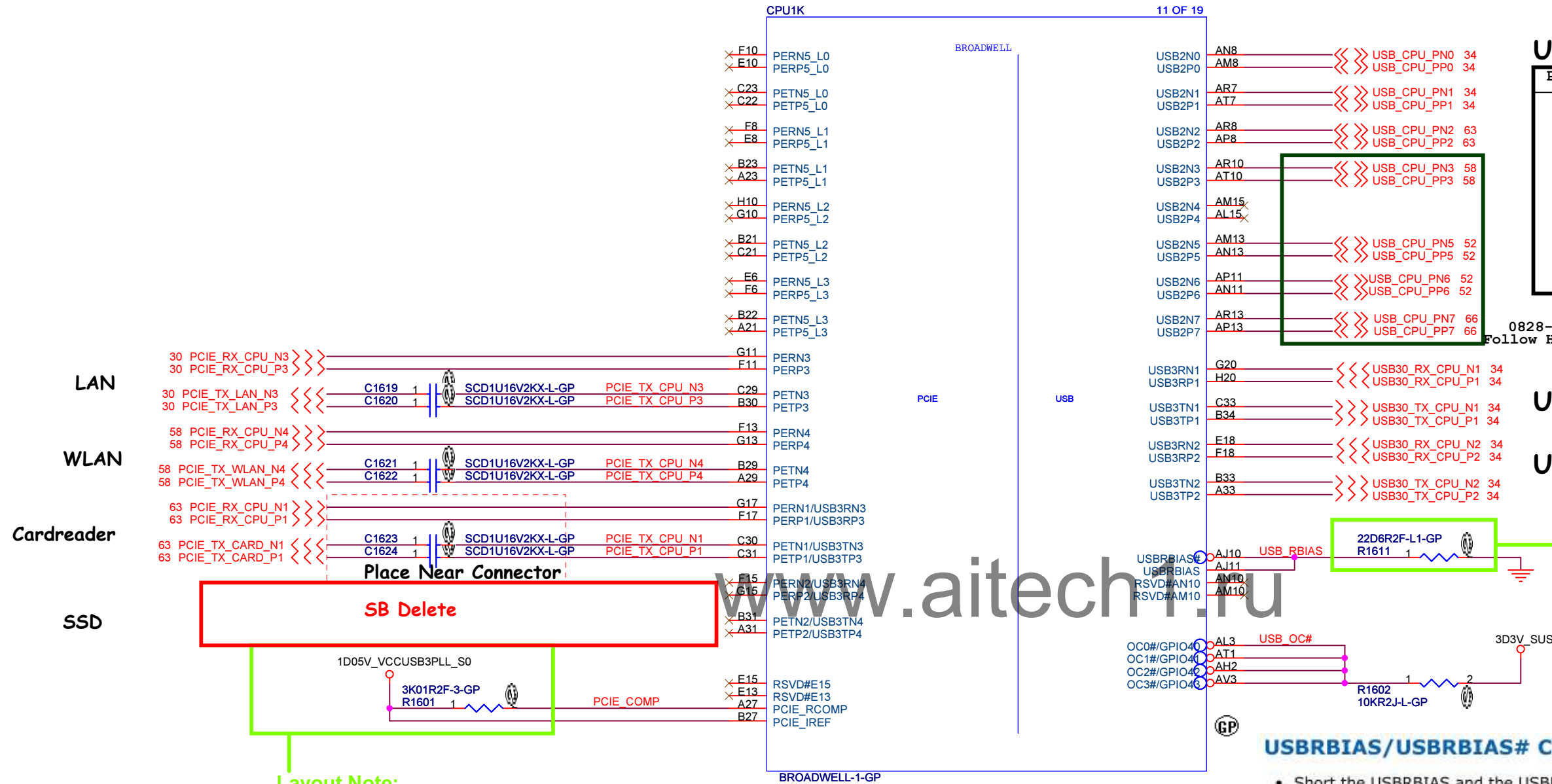
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SSID = CPU



SSID = PCH



Layout Note:

1. PCIE_RCOMP/ PCIE_IREF trace width=12~15mil
2. Isolation Spacing: 12mil
3. Total trace length<500mil

Signal	Trace Width	Isolation Spacing	Resistor Value	Length
PCIE_RCOMP	4 mils min (breakout) 12-15 mils (trace) Note: Must maintain low DC resistance routing (<0.2 ohm).	At least 12 mils to any adjacent high speed I/O.	3k ohm ±1% pulled to VCCUSB3PLL.	Max total = 500 mils
PCIE_IREF	4 mils min (breakout) 12-15 mils (trace) Note: Must maintain low DC resistance routing (<0.2 ohm).	At least 12 mils to any adjacent high speed I/O.	No resistor. Must connect directly to VCCUSB3PLL.	Max total = 500 mils

USB Table

Pair	Device
0	USB3.0 Port 1(CH6)
1	USB3.0 Port 2
2	USB2.0 Port 1(IO BD)
3	WLAN(Bluetooth)
4	N/A
5	Touch screen
6	CCD
7	Sensor Hub

0828-Ivan
Follow Hevin design

USB3.0

USB3.0

Layout Note:

1. USB_COMP using 50 ohm single-ended impedance
2. Isolation Spacing :15mil
3. Total trace length<500mil

USBRBIAS/USBRBIAS# Connection Guidelines

- Short the USBRBIAS and the USBRBIAS# pins at the package and then route on the top layer to one end of a 22.6 Ω ±1% resistor to ground (see Figure 15-2).
- Route signal using 50 ohm single-ended impedance and 500 mils (12.7-mm) max trace length and no longer than 450 mils to resistor.
- Avoid routing next to clock pins or under stitching capacitors. Recommended minimum spacing to other signal traces is 15 mils (0.381 mm).

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Title

CPU (PCI/USB)

Size

A3

Document Number

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Rev

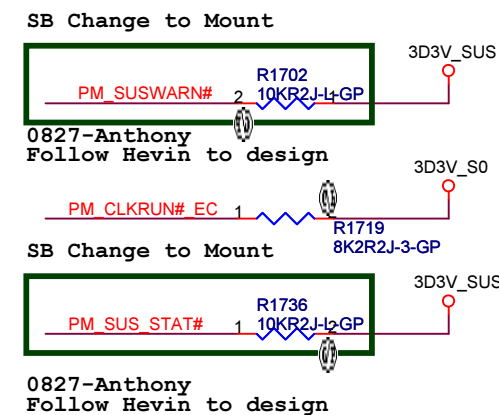
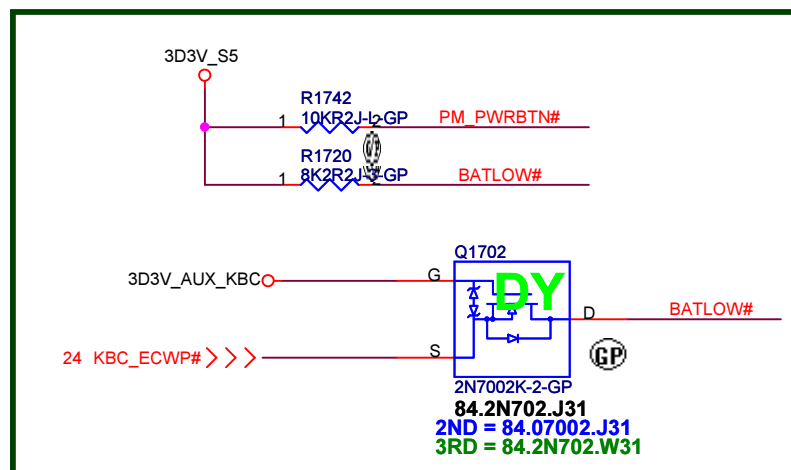
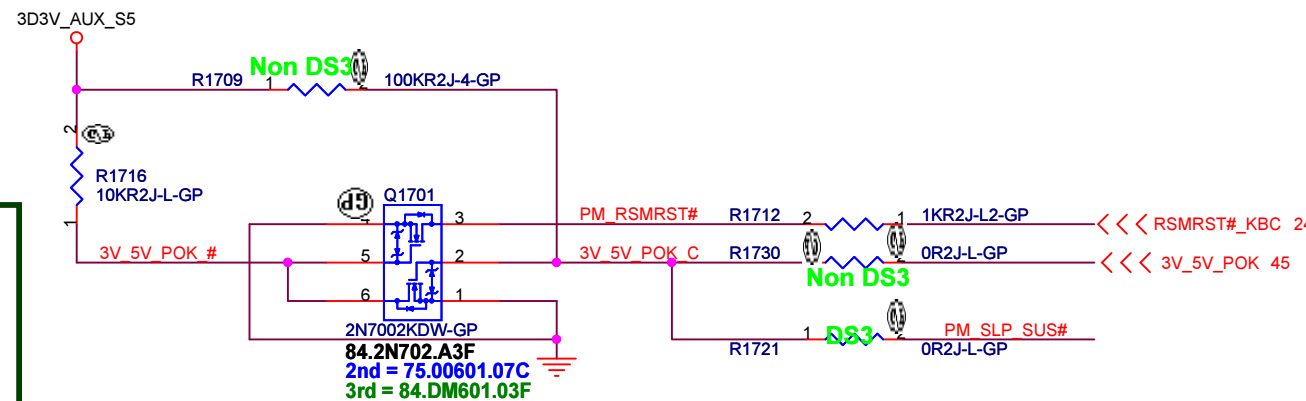
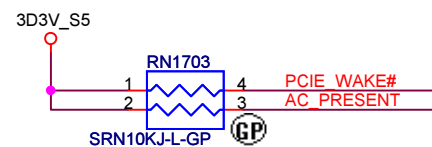
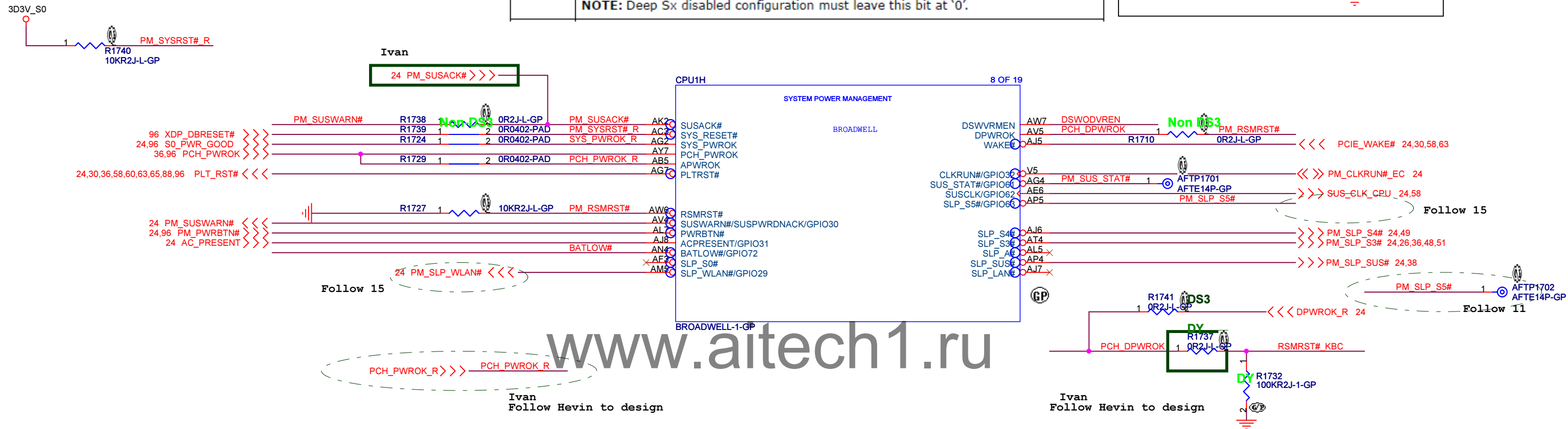
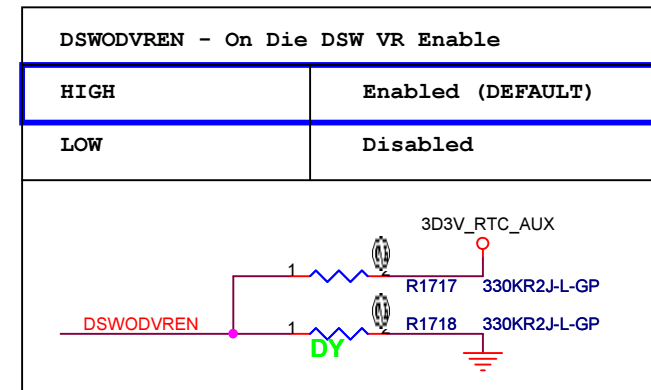
SA

Date: Monday, October 27, 2014

Sheet 16 of 102

SSID = CPU

Bit	Description
31:3	Reserved
2	WAKE# Pin Deep Sx Enable (WAKE_PIN__DSX_EN) - R/W. When this bit is '1', the PCI Express WAKE# pin is monitored while in Deep Sx, supporting wake from Deep Sx due to assertion of this pin. In this case the platform must externally pull-up the pin to the DSW (instead of pulling-up to the SUS as historically been the case). When this bit is '0': <ul style="list-style-type: none">Deep Sx configurations: The PCH internal pull-down on the WAKE# pin is enabled in Deep Sx and during G3 exit and the pin is not monitored during this time.Deep Sx disabled configurations: The PCH internal pull-down on the WAKE# pin is never enabled. NOTE: Deep Sx disabled configuration must leave this bit at '0'.

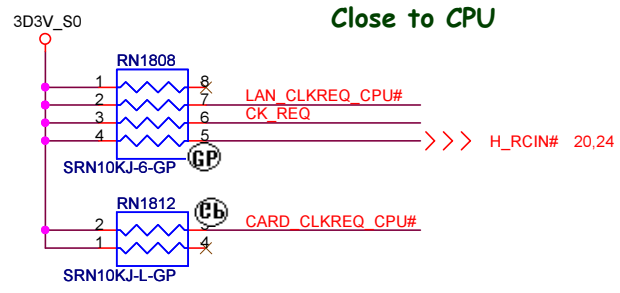


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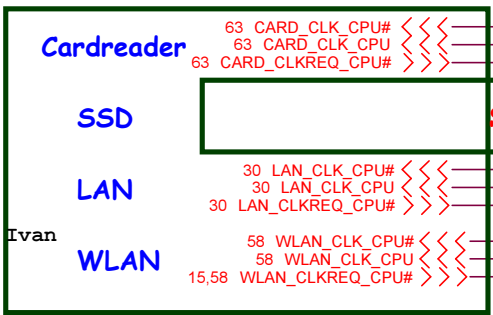
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SSID = CPU

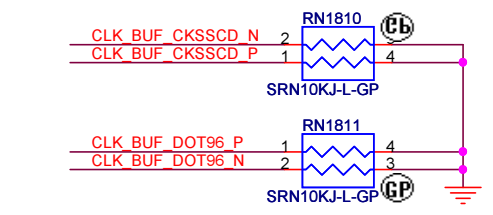
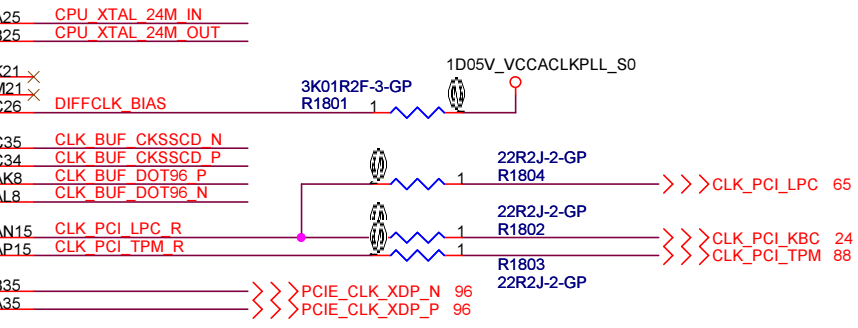
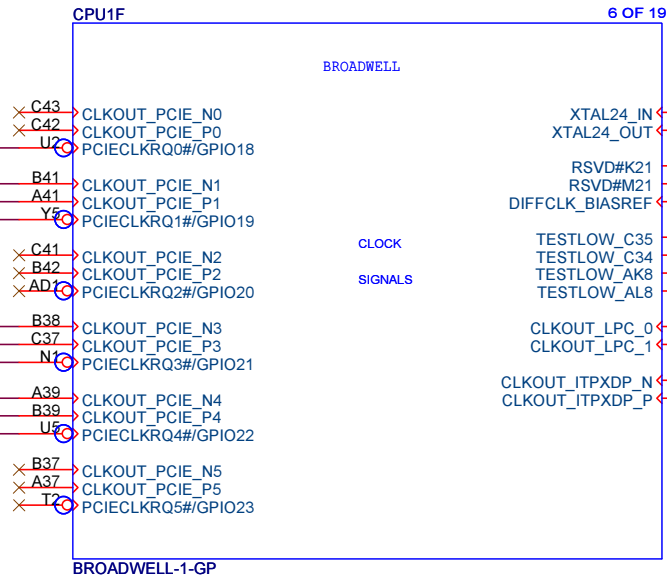
Close to CPU



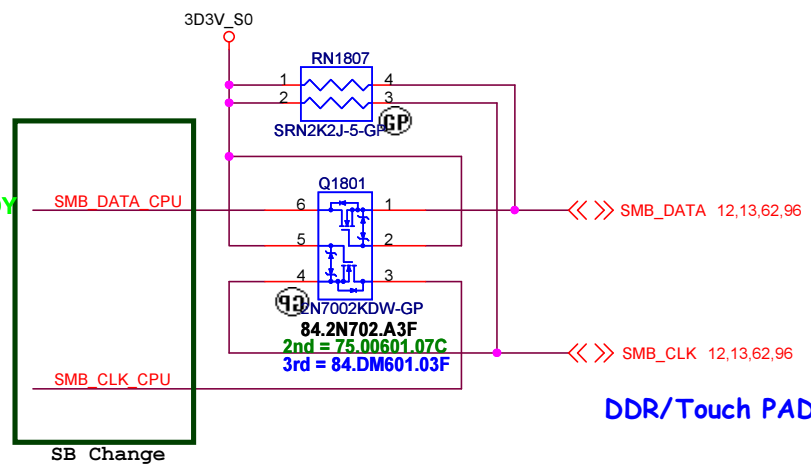
Follow 15



SB Delete

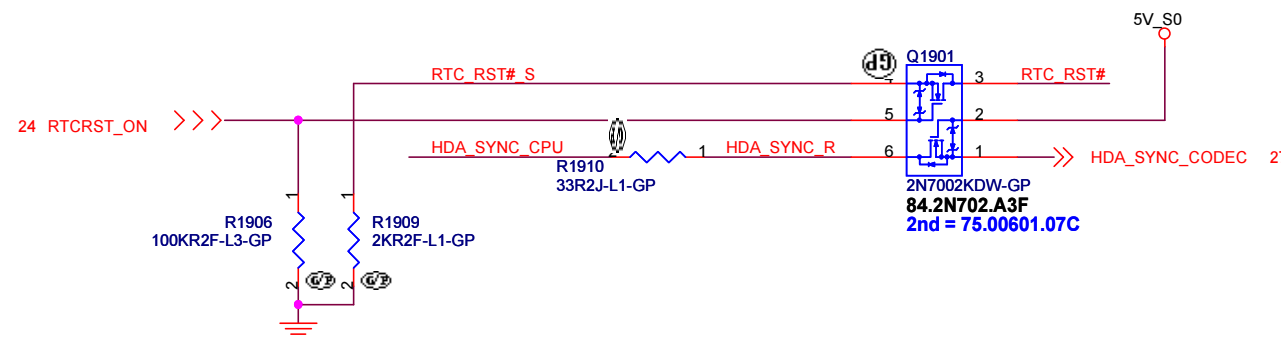
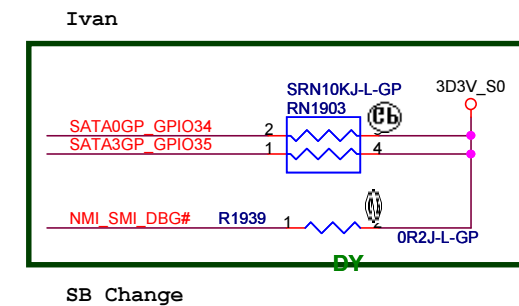
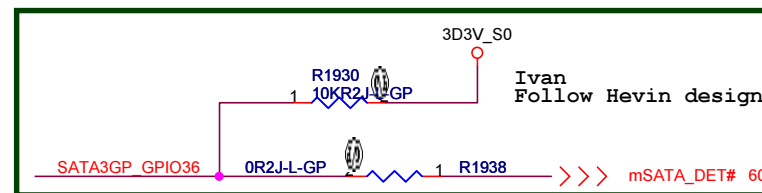
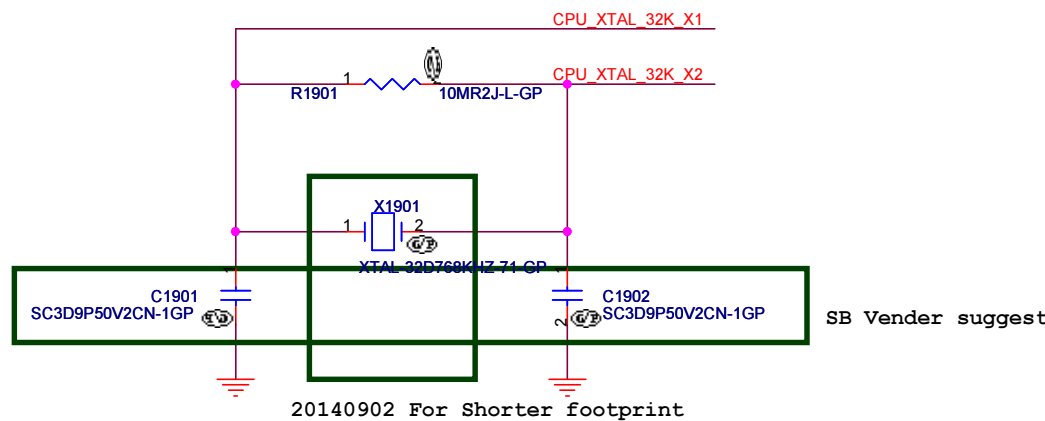
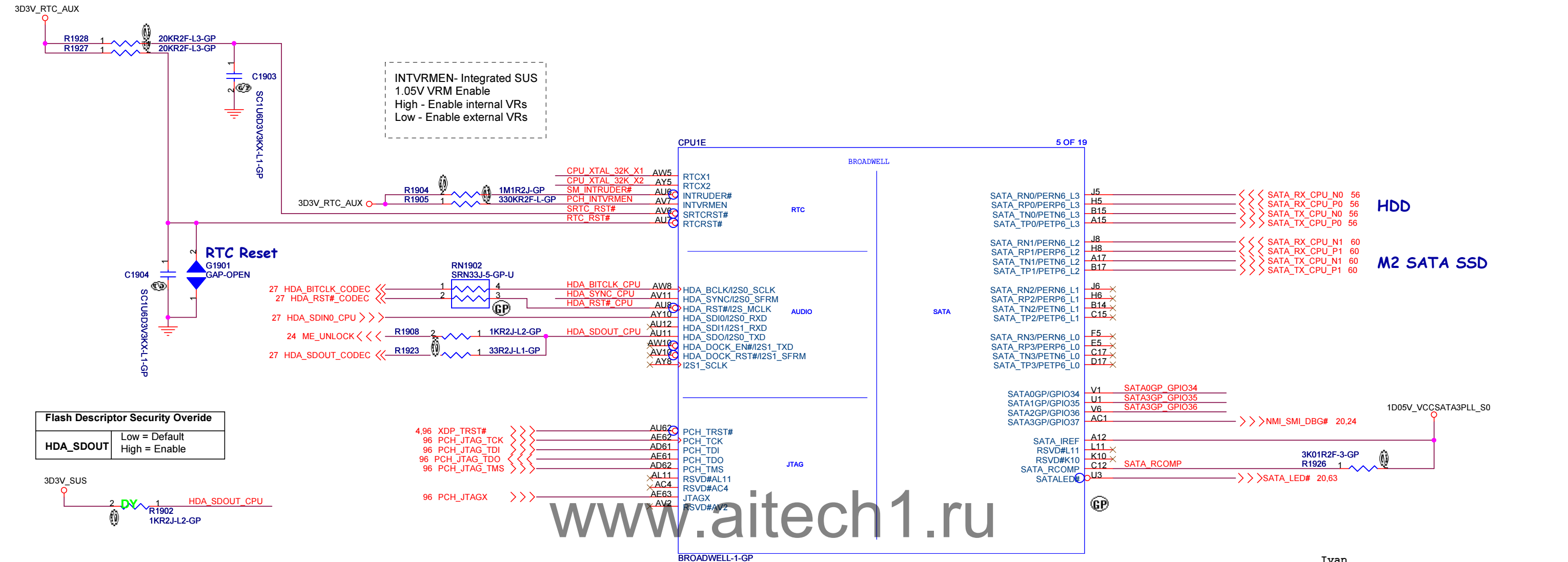


Need very close to CPU



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SSID = CPU



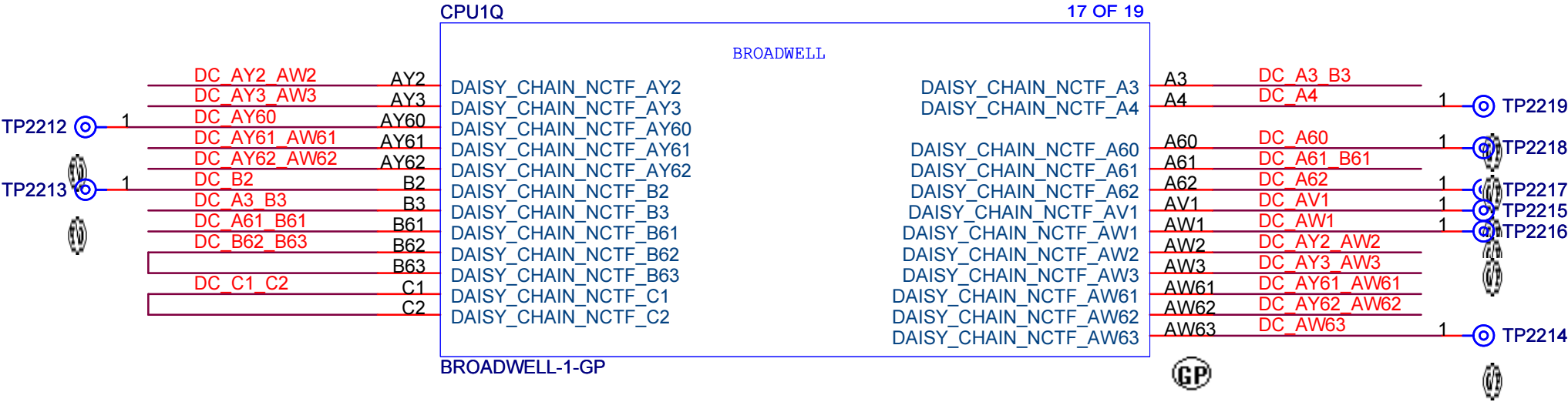
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Title		
CPU (RTC/LPC/SATA/HDA)		
Size	Document Number	Rev
Custom	Fauchon-BDW 13"	SA
Date:	Monday, November 03, 2014	Sheet 19 of 102

SSID = CPU



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Title			
CPU (RSVD)			
Size	Document Number		Rev
A4	Fauchon-BDW 13"		SA
Date:	Saturday, September 13, 2014		Sheet 22 of 102

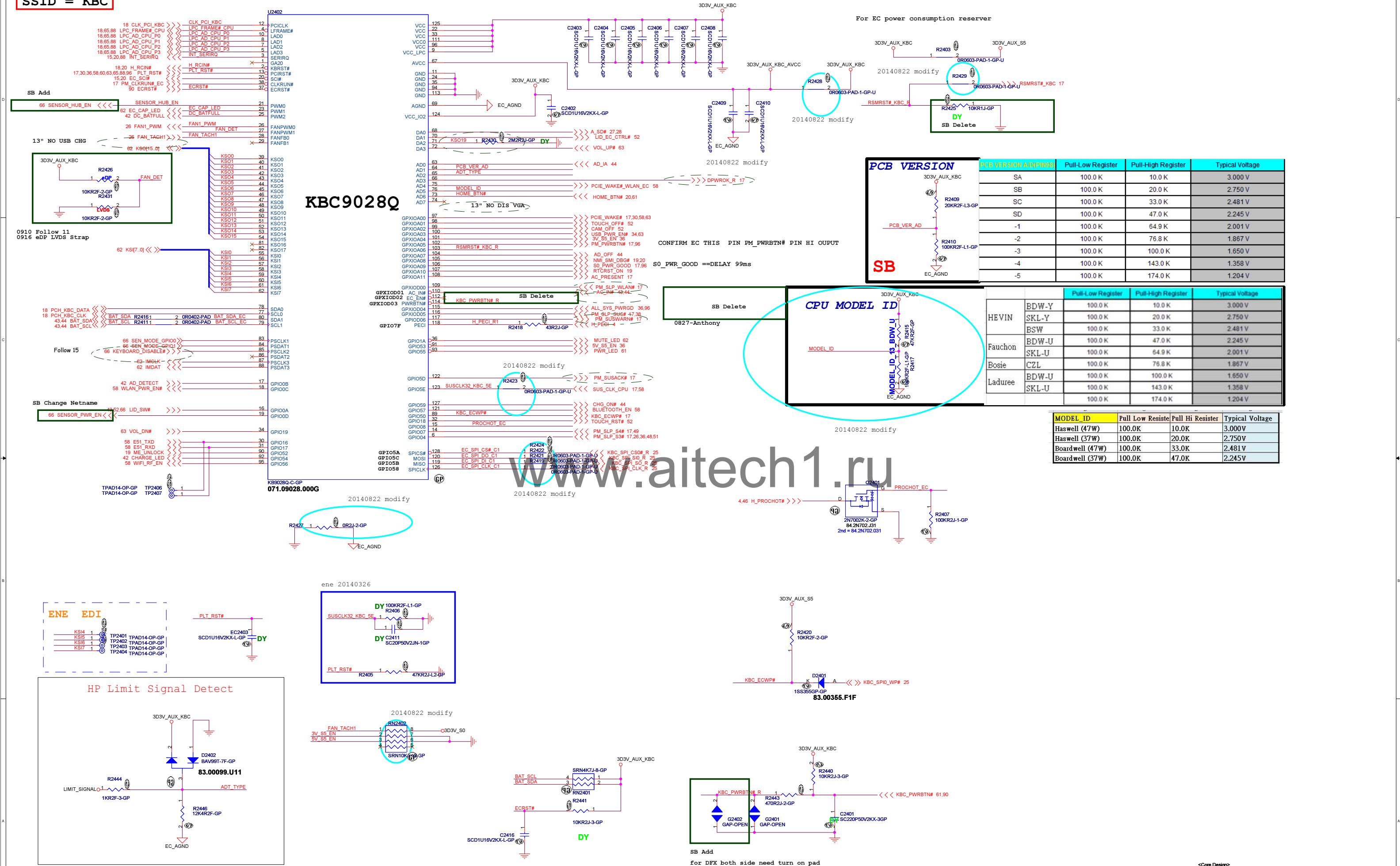
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Size A4	Document Number Fauchon-BDW 13"		Rev SA
Date: Saturday, September 13, 2014	Sheet 23	of	102

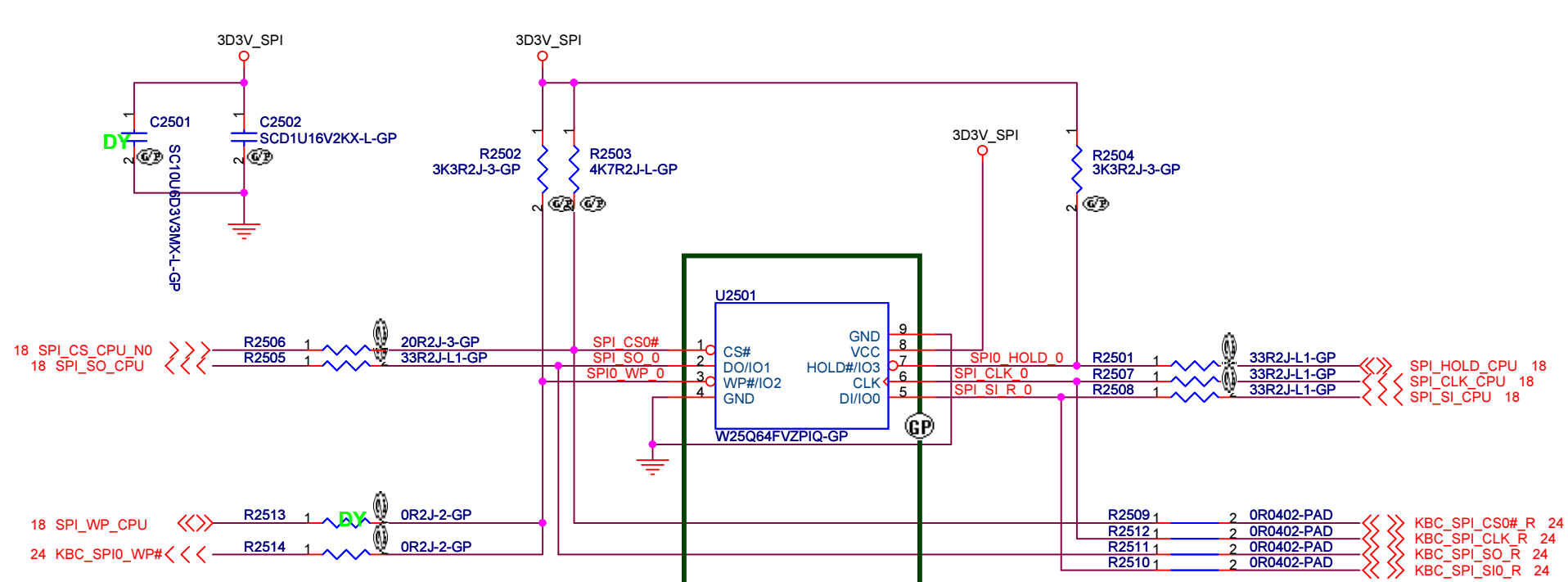
SSID = KBC



SSID = Flash.ROM

SPI FLASH ROM (8M byte) for PCH

SPI ROM Equal length need to less than 500mil

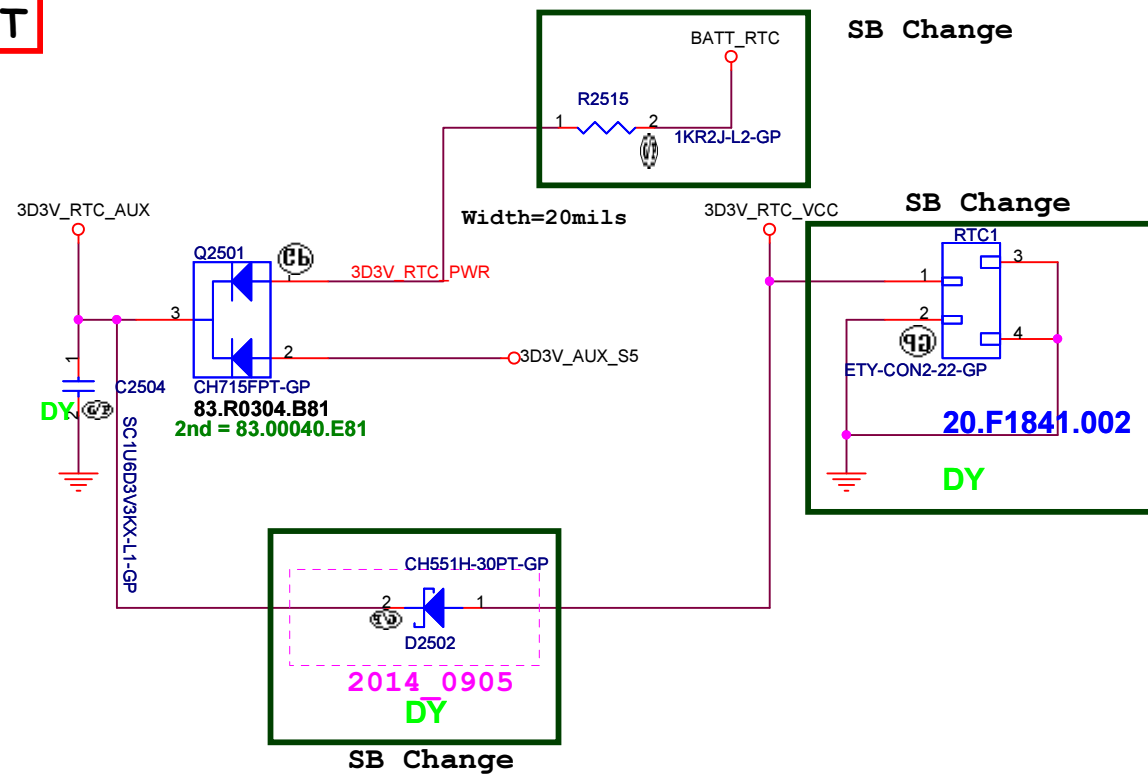


SB Change PN

Del SKT

SB Change PN
Del SKT

SSID = RBAT



EV

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Title

Flash(KBC+PCH)/RTC

Size
A3

Document Number

Fauchon-BDW 13"

SA

Date: Monday, November 03, 2014

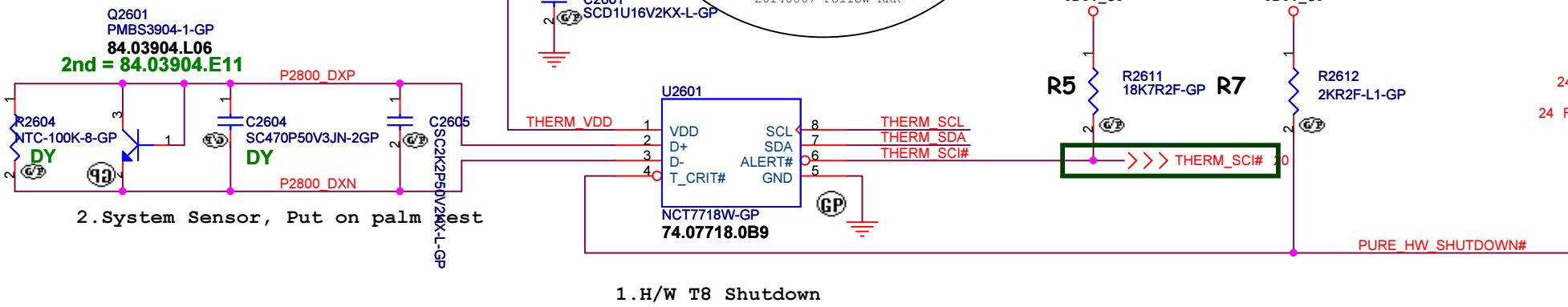
Sheet 25 of

02

SSID = Thermal

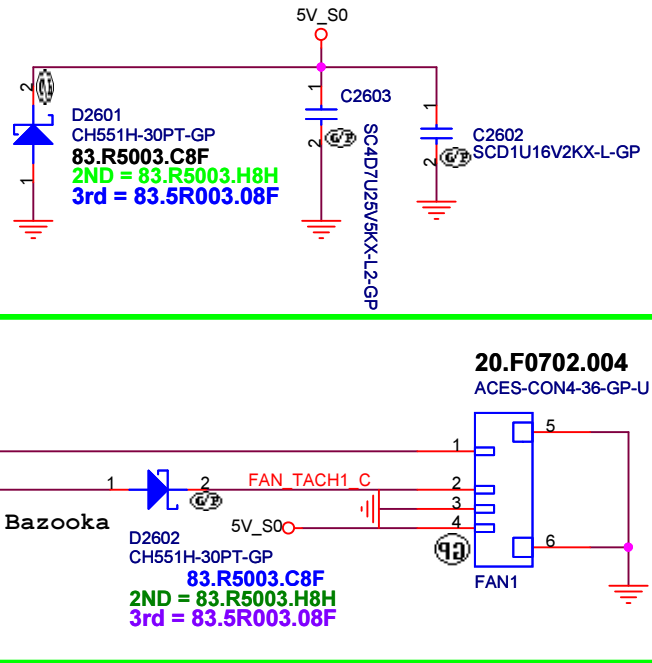
Thermal sensor NCT 7718W

Layout notice :
Both DXN and DXP routing 10 mil
trace width and 10 mil spacing.



Layout 15 mil

SB Corrected
SML1_DATA 18
SML1_CLK 18



NCT7718W I2C/ SMBus™ address is 1001100xb (x is R/W bit).

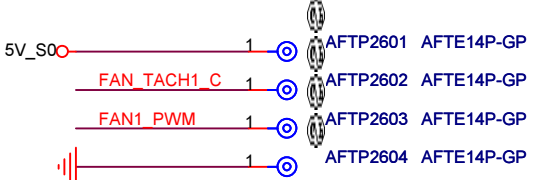
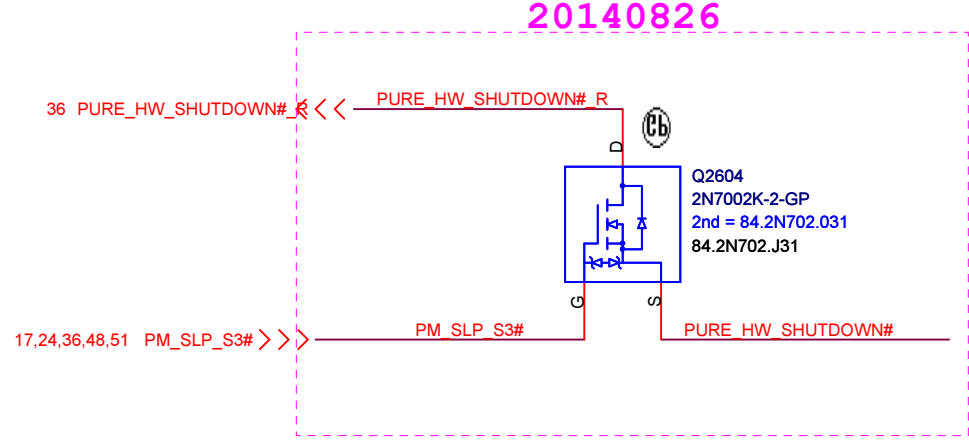
98 / 4C

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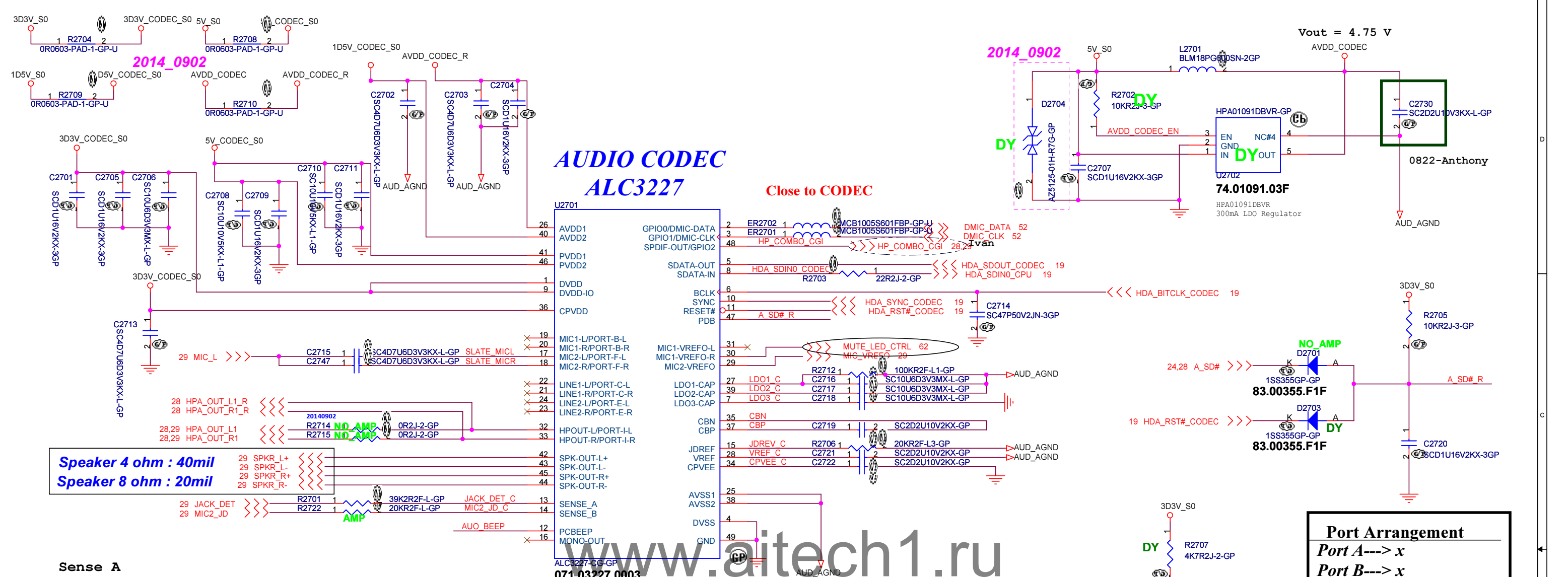
ALERT# /T CRIT#
Pull-up Resistor

	2Kohm	7.5Kohm	10.5Kohm	14Kohm	18.7Kohm
R5	77°C	87°C	97°C	107°C	117°C
	79°C	89°C	99°C	109°C	119°C
	81°C	91°C	101°C	111°C	121°C
	83°C	93°C	103°C	113°C	123°C
	85°C	95°C	105°C	115°C	125°C

T_CRIT temperature strapping point



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Speaker 4 ohm : 40mil
Speaker 8 ohm : 20mil

Sense A
10K ohm for LINE1 (Port C)
20K ohm for MIC1 (Port B)
39.2K ohm for HP-Out (Port I)

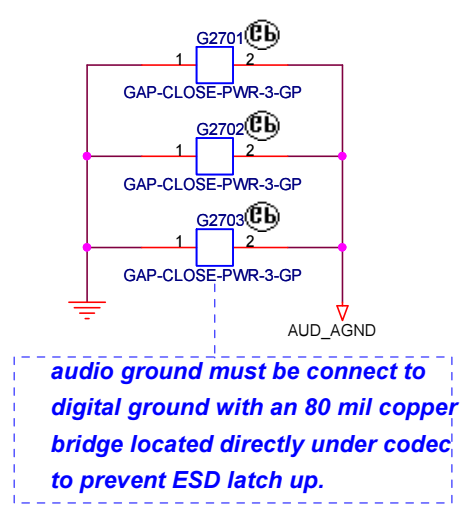
Sense B
10K ohm for FRONT (Port D)
20K ohm for MIC2 (Port F)
39.2K ohm for LINE2 (Port E)

Port Arrangement

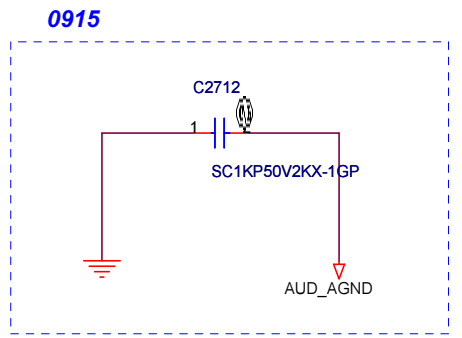
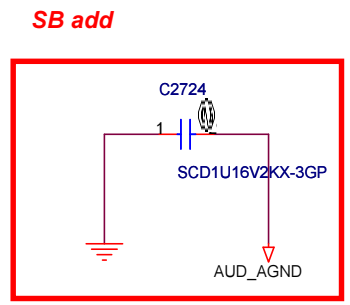
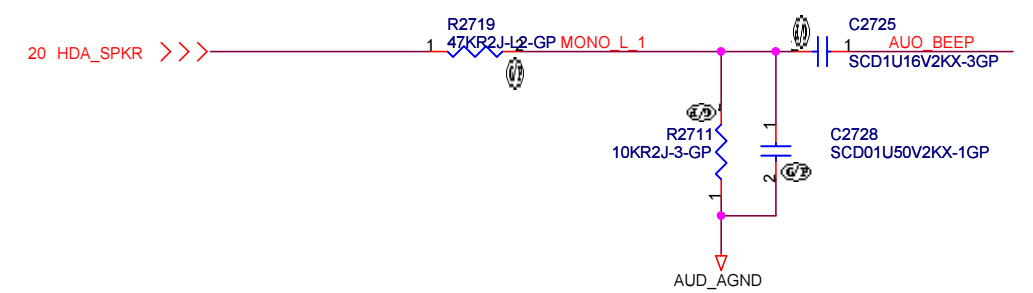
Port A---> x
Port B---> x
Port C---> x
Port D---> Speaker
Port E---> x
Port F---> Mic In
Port G---> x
Port H---> x
Port I---> Head Phone

Digital GND & AUD_AGND

Tie Analog GND and Digital GND under codec by a single point



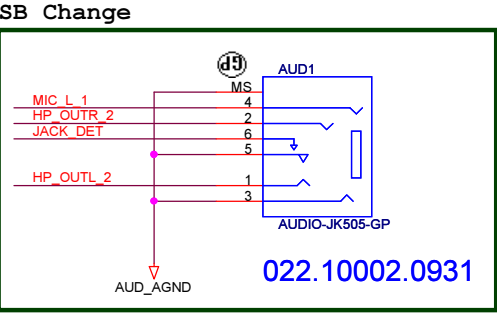
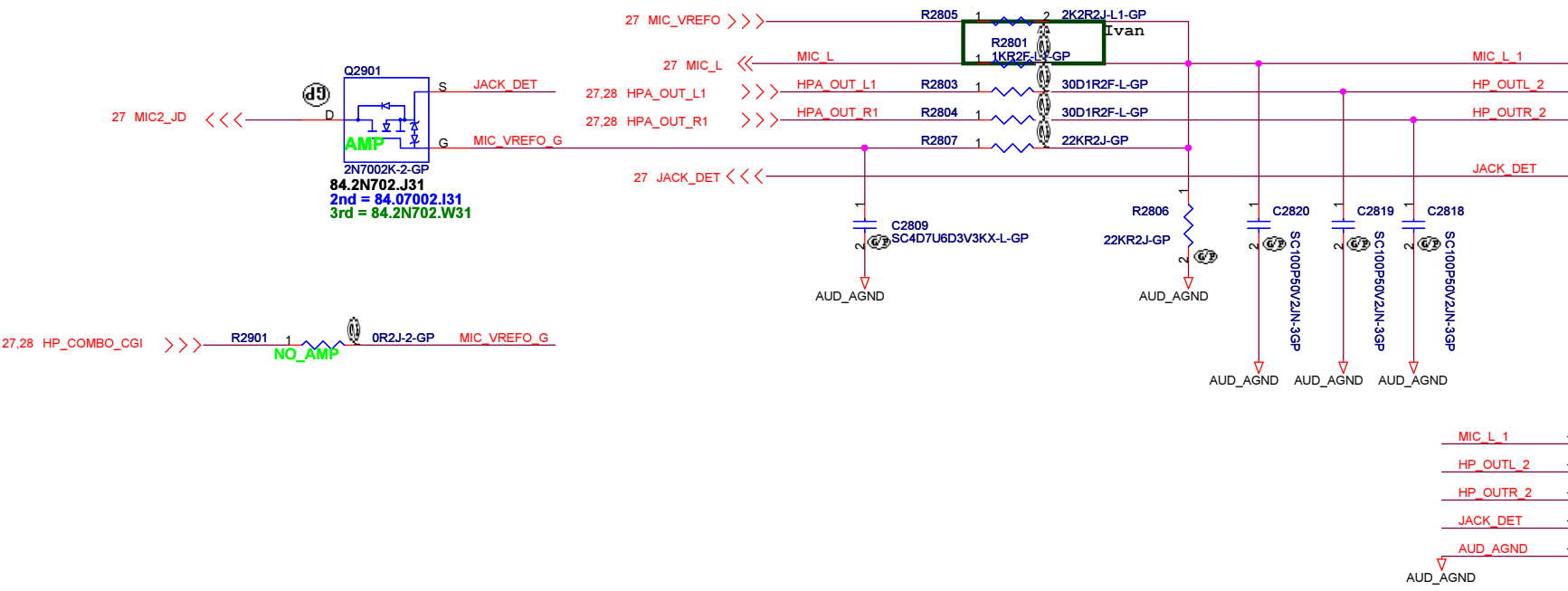
PC BEEP



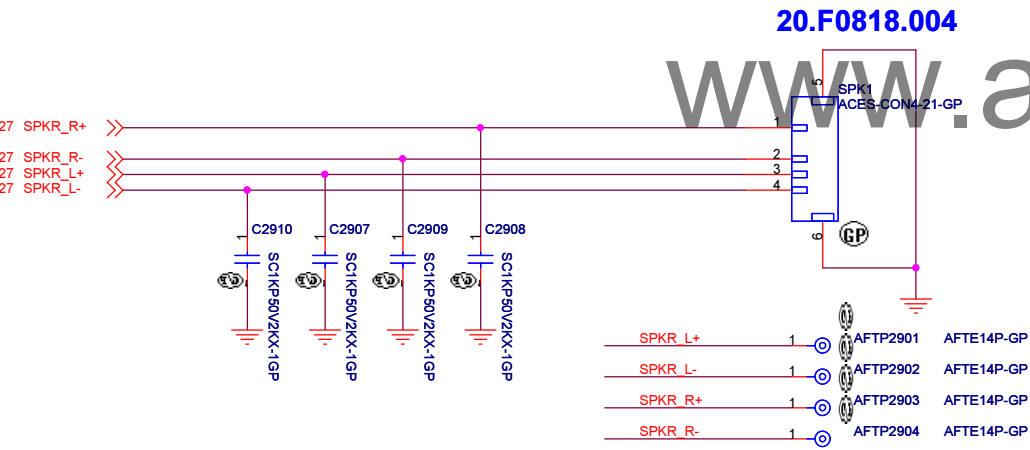


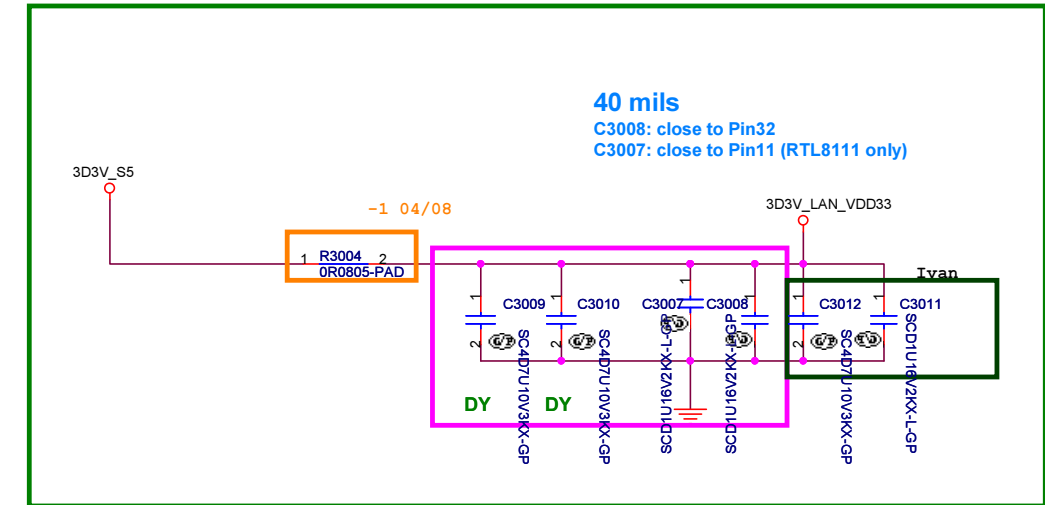
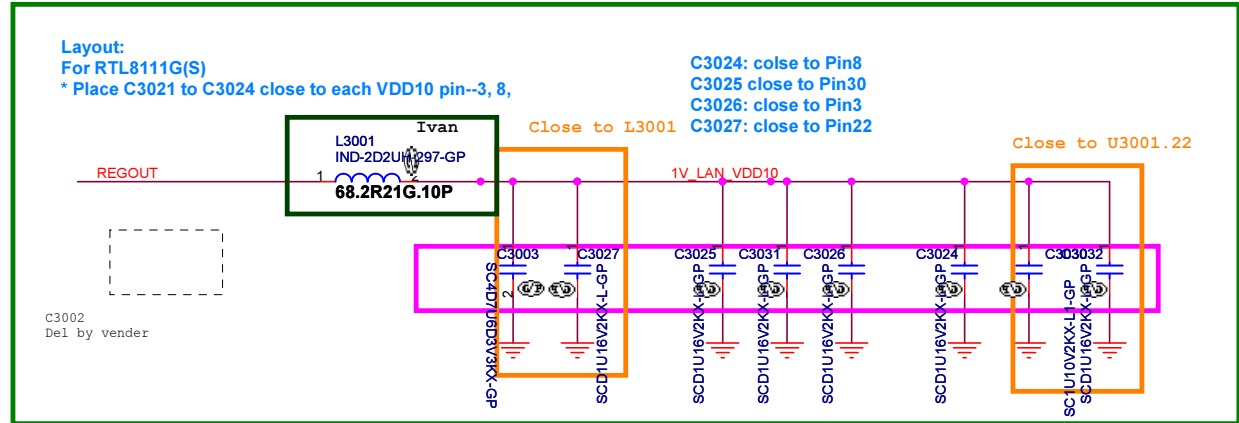
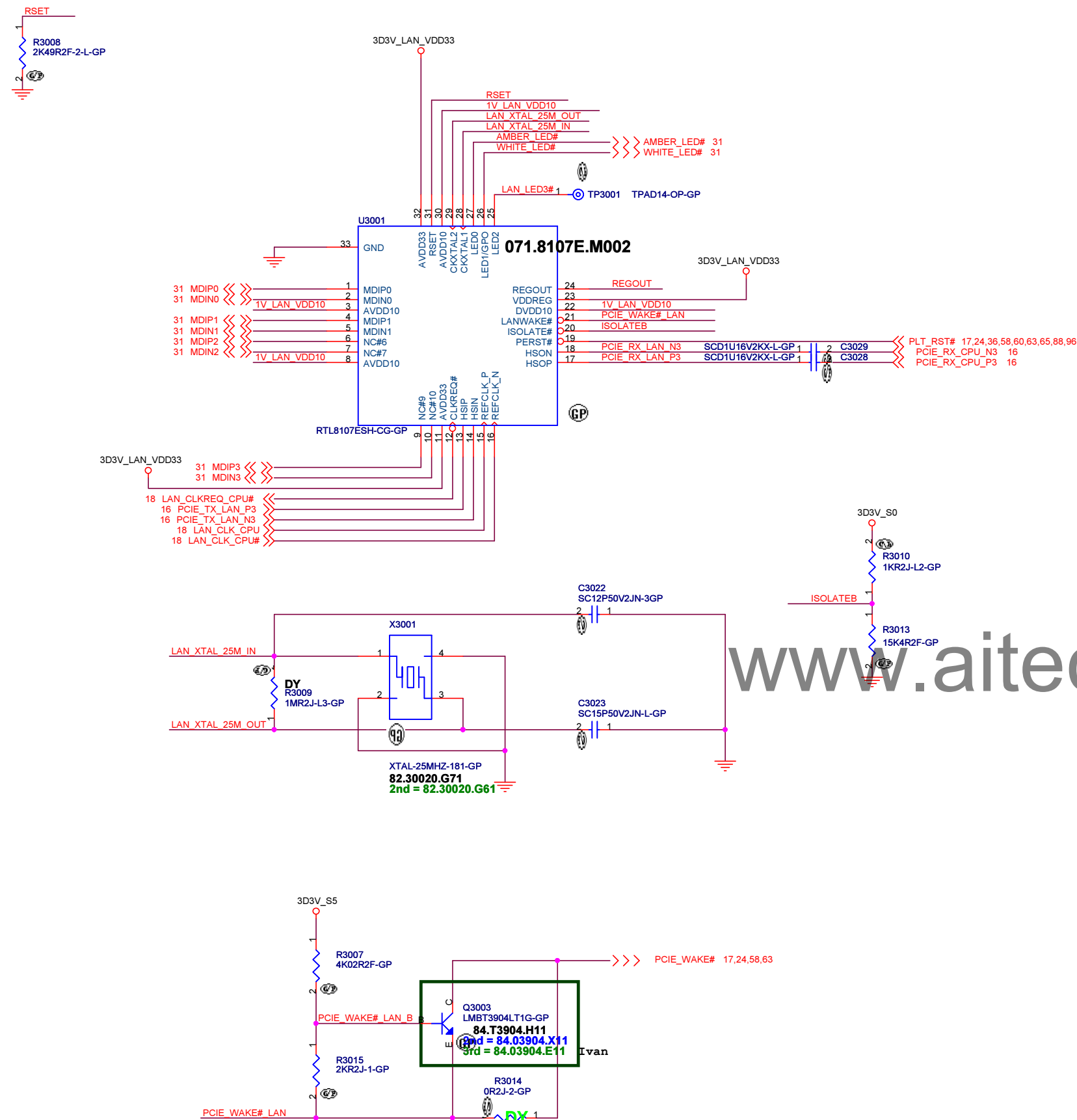
AUDIO COMBO JACK

Combo-Jack (Headphone & MIC)



Speaker



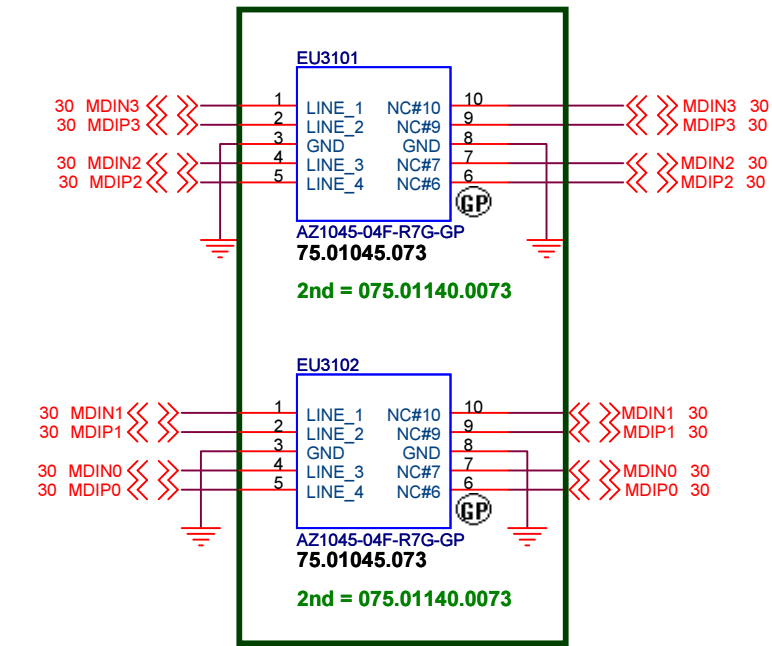


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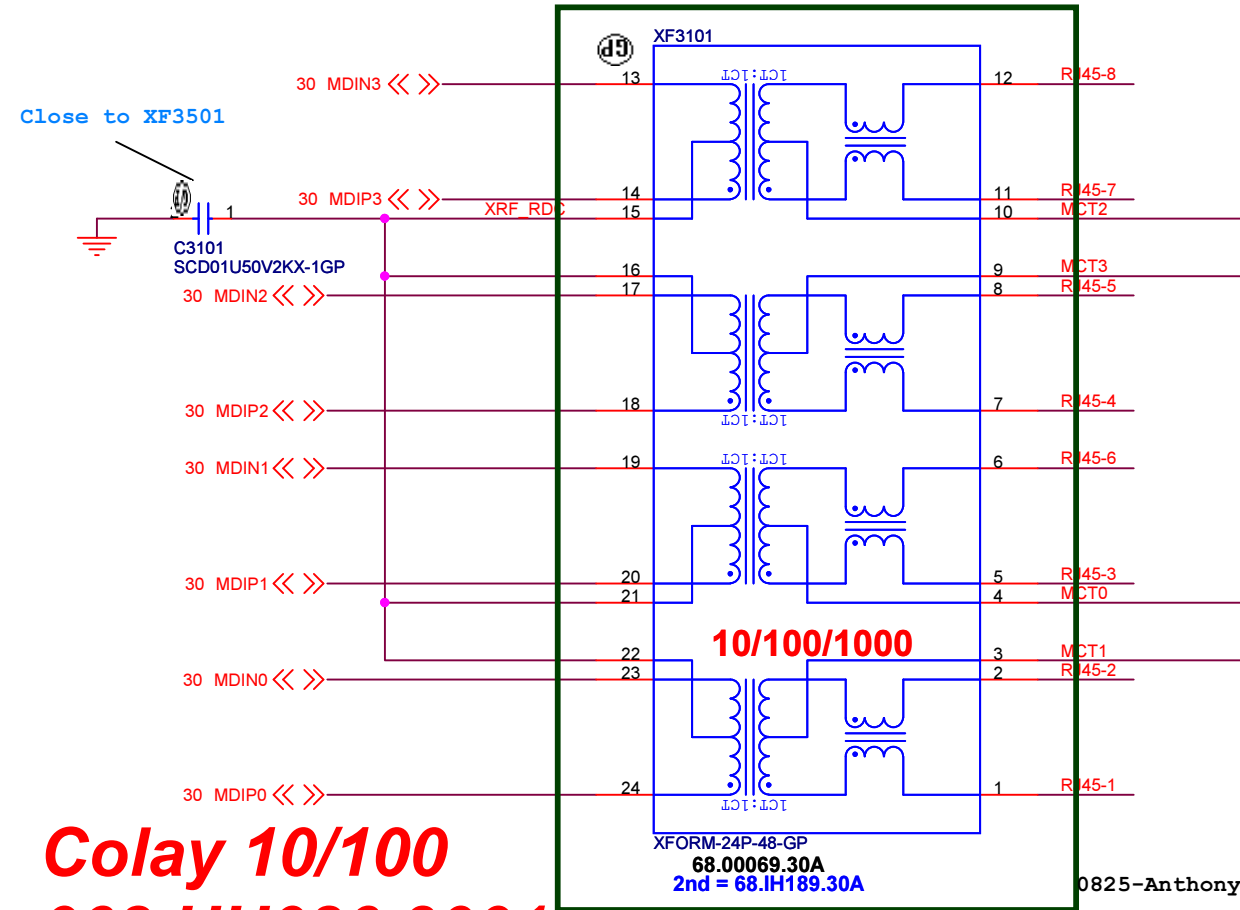
EV

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Title LAN(RTL8107/RTL8111)	
Size Custom	Document Number Fauchon-BDW 13"
Date: Monday, October 27, 2014	Rev SA
Sheet 30 of 102	

SSID = LOM



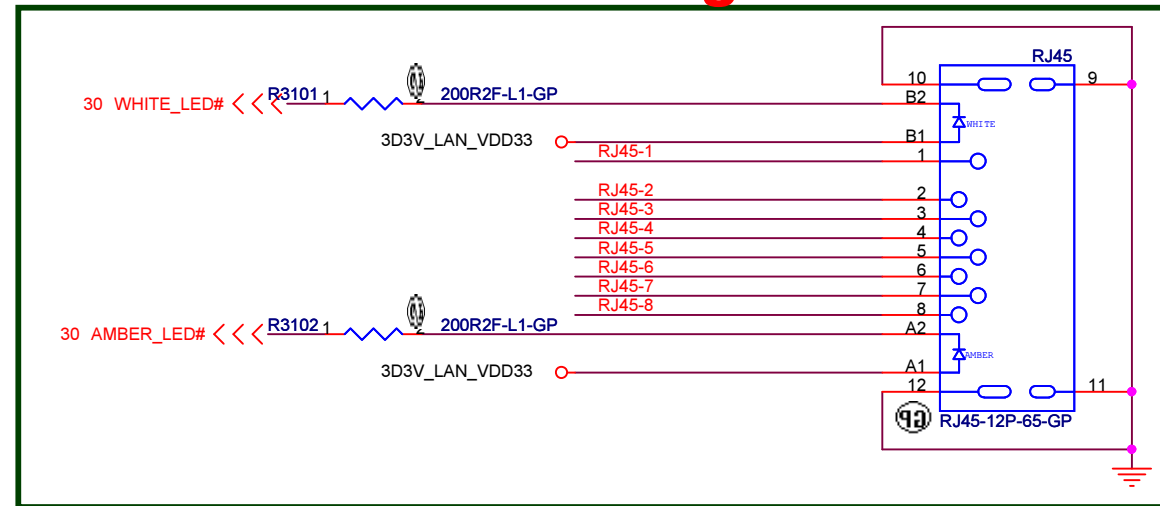
SB Add



Colay 10/100
068.HH086.3001

RJ45 Connector

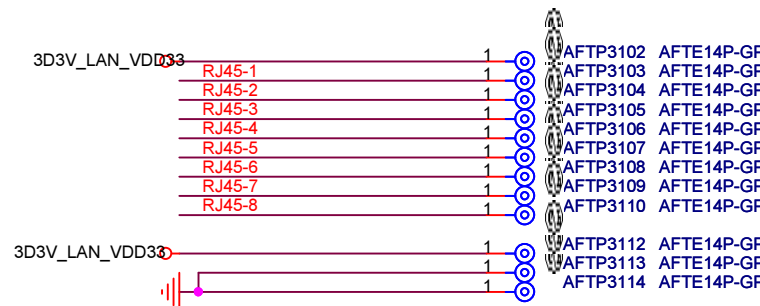
SB Change



wavelength : Orange 605mm need check

- Green 10(+), 9(-)
- YELLOW 12(+), 13(-)
- (1) route on bottom as differential pairs.
 - (2) Tx+/Tx- are pairs. Rx+/Rx- are pairs.
 - (3) No vias, No 90 degree bends.
 - (4) pairs must be equal lengths.
 - (5) 6mil trace width, 12mil separation.
 - (6) 36mil between pairs and any other trace.
 - (7) Must not cross ground moat, except RJ-45 moat.

SB EMI Delete



EV

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Taipei Hsien 221, Taiwan, R.O.C.

Title (LAN+VGA) CONNECTOR
Size A3 Document Number Fauchon-BDW 13"
Date: Monday, October 27, 2014 Sheet 31 of 102 Rev SA



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EV

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Title <div>RTS5237(CARD READER)</div>	
Size <div>A4</div>	Document Number <div>Fauchon-BDW 13"</div>
Date: Saturday, September 13, 2014	Rev <div>SA</div>
Sheet 32 of 102	

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EV

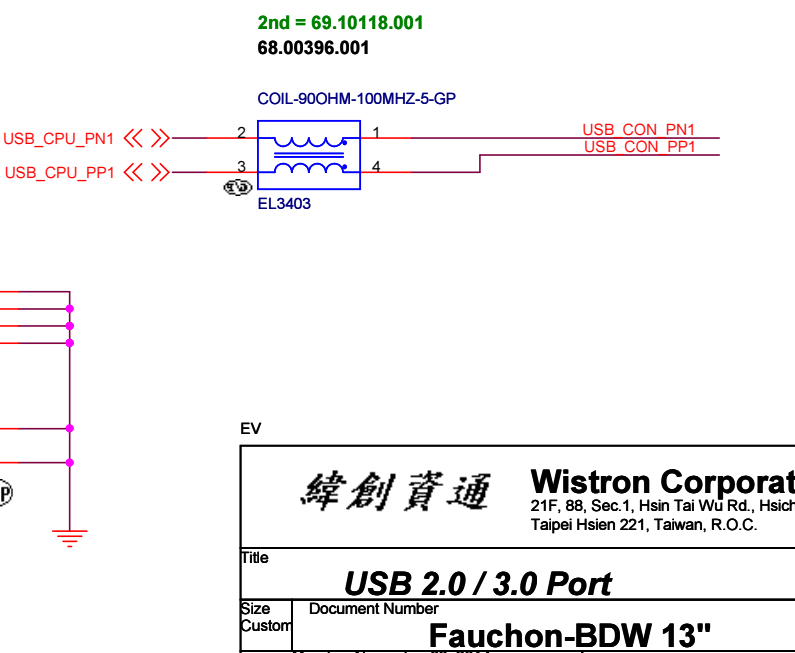
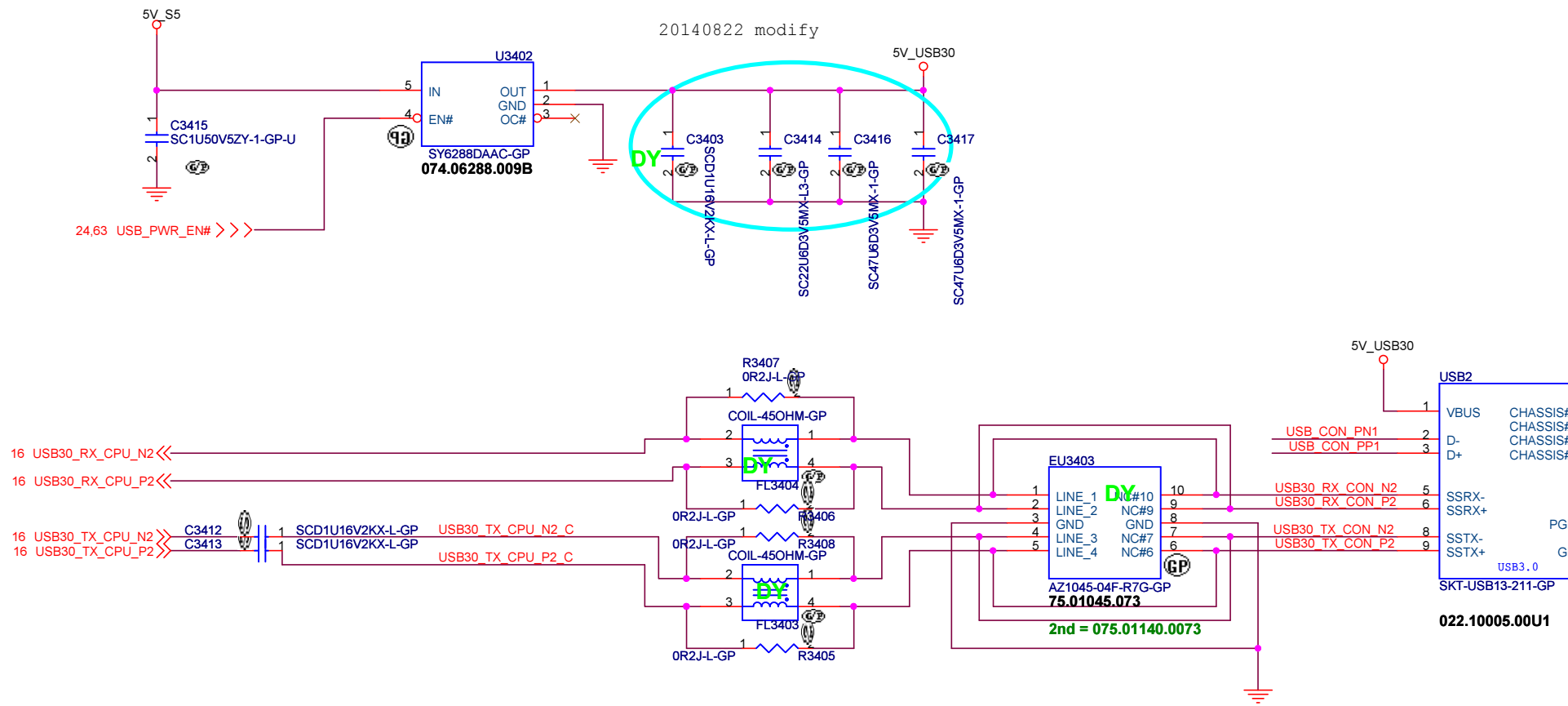
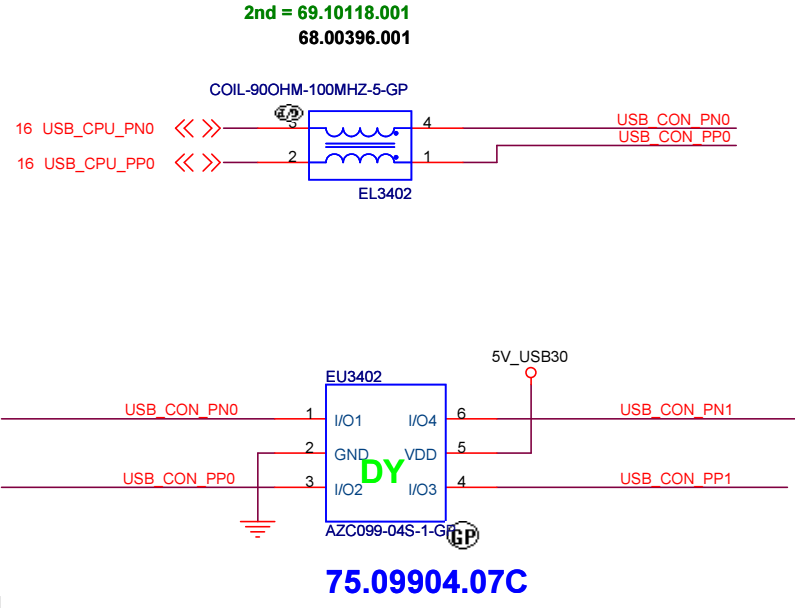
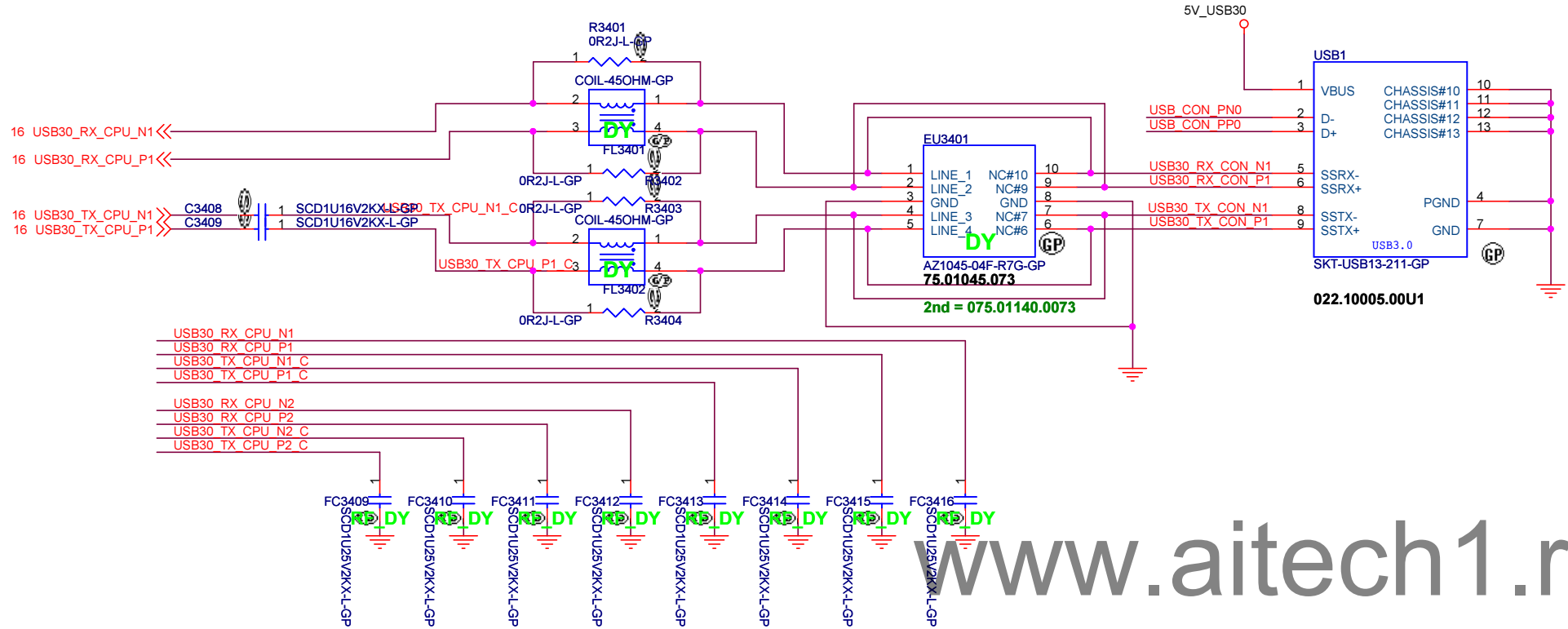
<div><div>緯創資通</div><div>Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div></div>		
Title		
CARD Reader CONN		
Size	Document Number	Rev
A3	Fauchon-BDW 13"	SA
Date:	Saturday, September 13, 2014	Sheet 33 of 102

USB Table

Pair	Device
0	USB3.0 Port 1
1	USB3.0 Port 2
2	USB2.0 Port 3
3	Sensor Hub
4	WLAN(Bluetooth)
5	Touch screen
6	CCD
7	

USB 3.0 Connector
Pin definition

1	POWER
2	USB 2.0 D-
3	USB 2.0 D+
4	GND
5	StdA_SSRX- SuperSpeed RX
6	StdA_SSRX+
7	GND
8	StdA_SSTX- SuperSpeed TX
9	StdA_SSTX+



5

4

3

2

1

D

D

C

C

B


B

A

A

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MB

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Title			
USB CHARGER			
Size	Document Number		Rev
A4	Fauchon-BDW 13"		SA
Date:	Saturday, September 13, 2014		Sheet 35 of 102

5

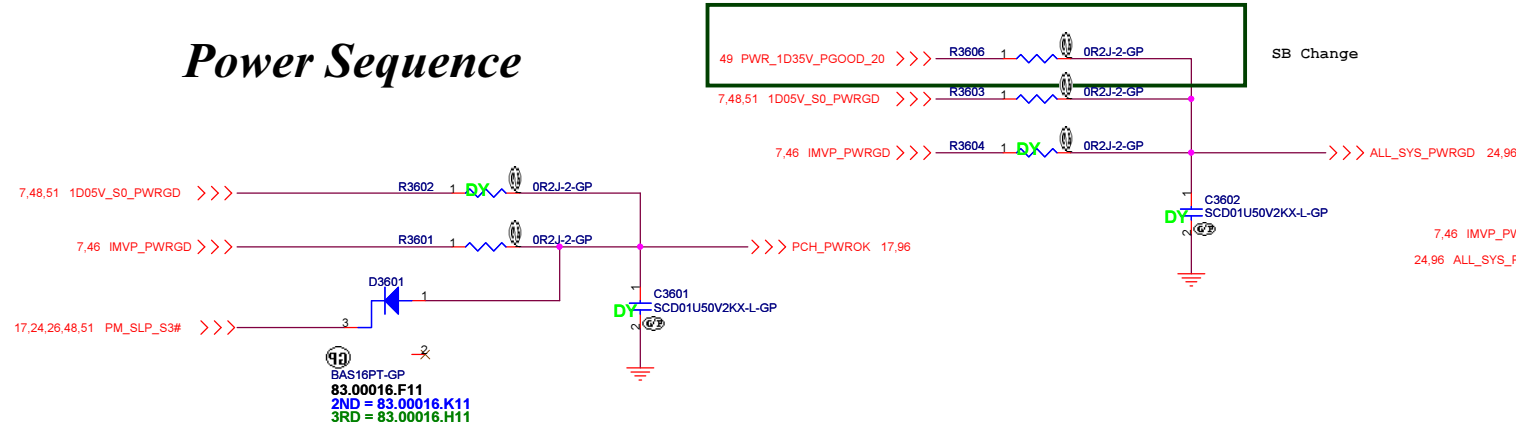
4

3

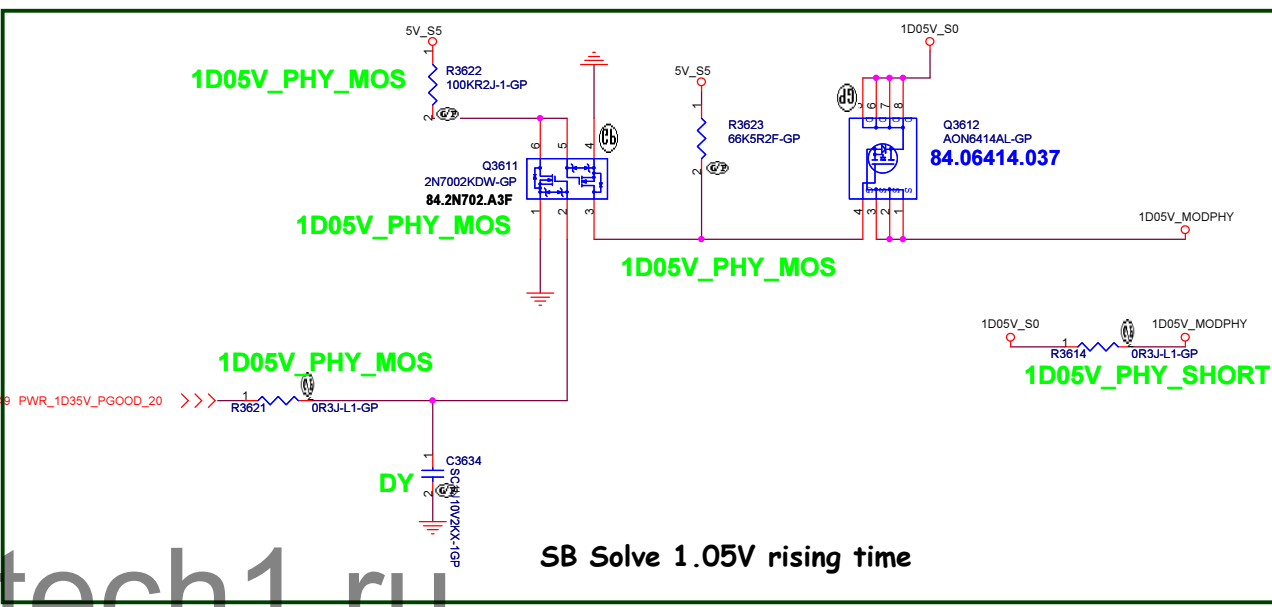
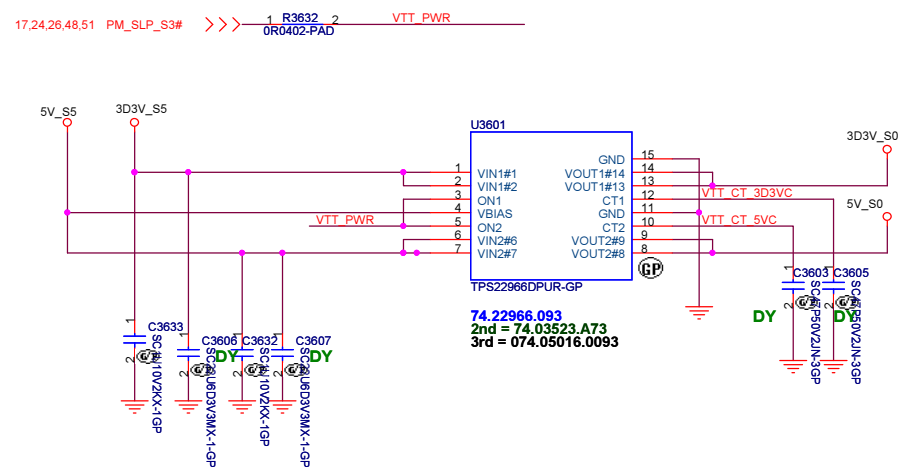
2

1

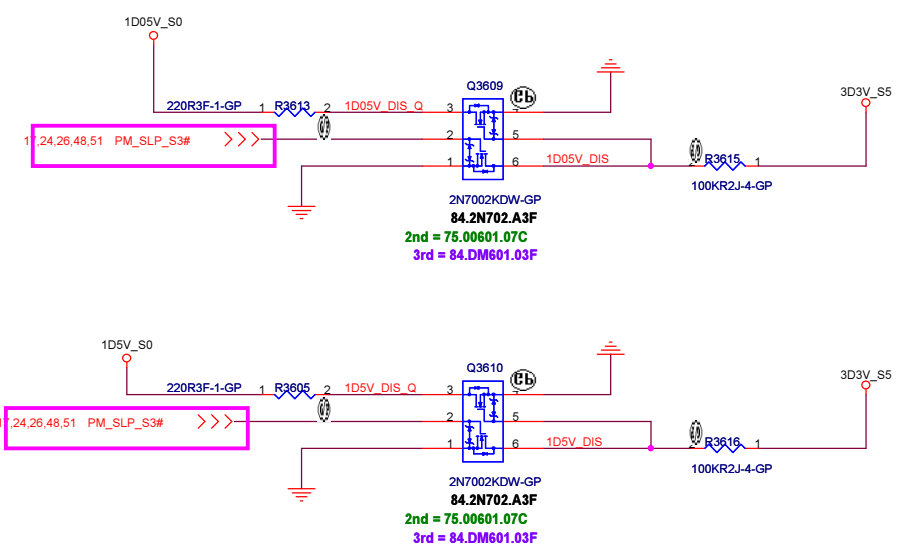
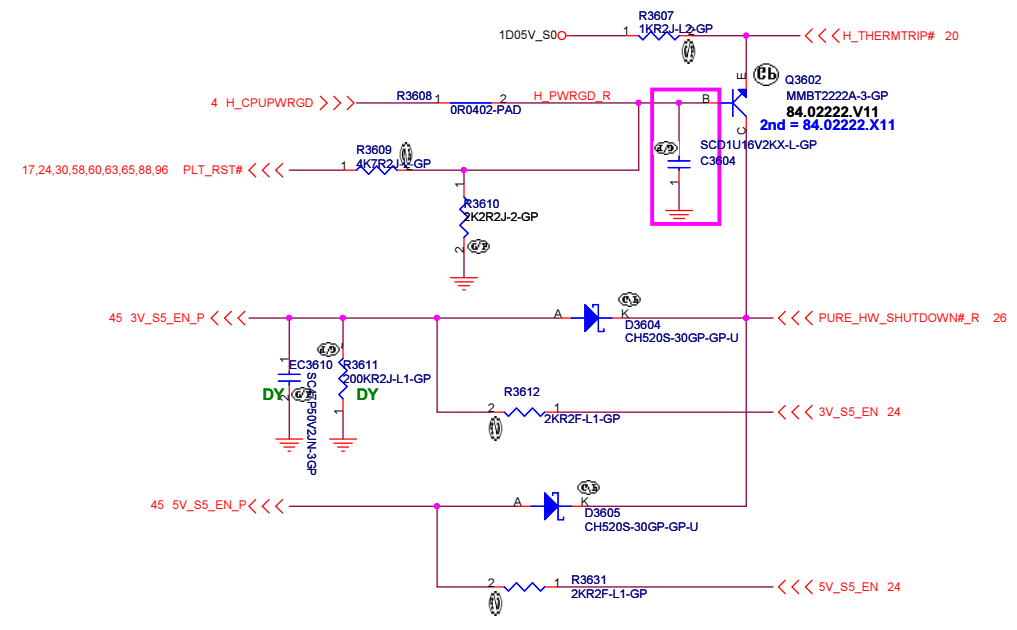
Power Sequence



Run Power



Discharge circuit



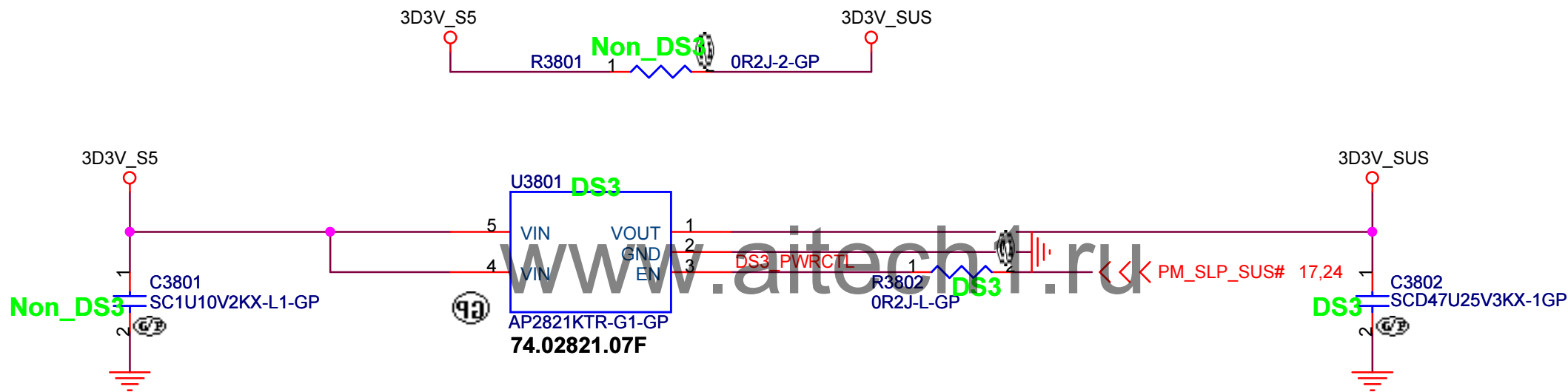
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D				D
C				C
B				B
A				A

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Title			
ADAPTER OCP / S3 reduction			
Size	Document Number		Rev
Custom	Fauchon-BDW 13"		SA
Date:	Saturday, September 13, 2014	Sheet 37 of	102



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Title	
DS3	
Size A4	Document Number Fauchon-BDW 13"
	Rev SA
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Power Sequence

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Title

1D05 M

Size Custom

Document Number

Rev

Fauchon-BDW 13"

SA

Date: Saturday, September 13, 2014

Sheet 39 of 102

5					4					3					2					1				
D																				D				
C																				C				
→																				←				
B																				B				
A																				A				

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Title

Connected Standby1

Size
A

Document Number
Fauchon-BDW 13"

Rev
SA

Date: Saturday, September 13, 2014Sheet 40 of 102

5	4	3	2	1
D				D
C				C
B				B
A				A

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Title

Connected Standby2

Size
A

Document Number

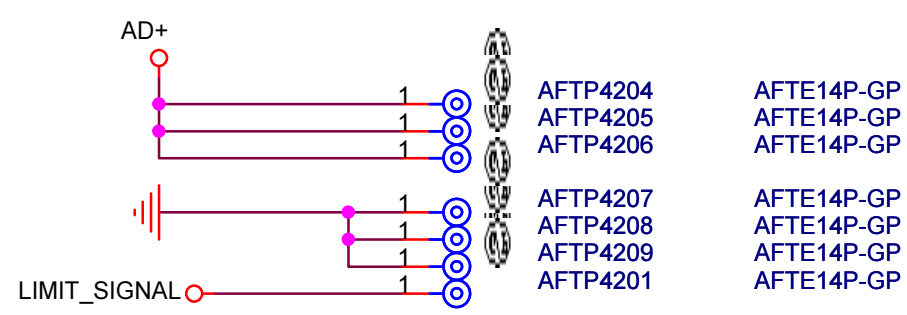
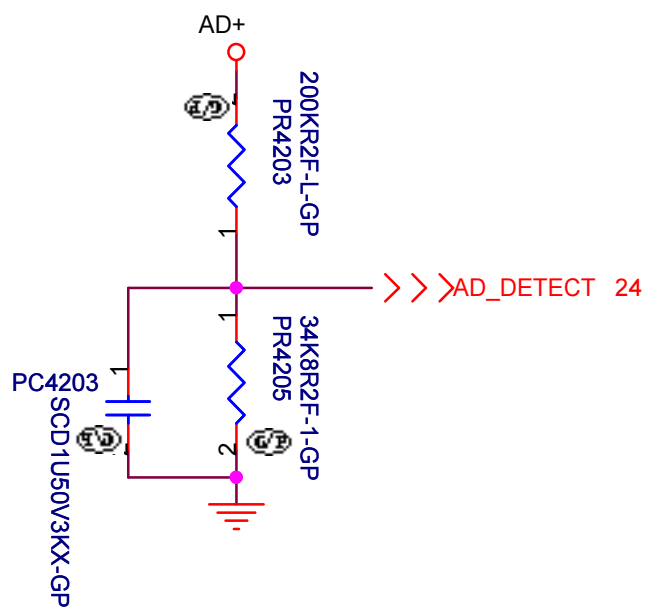
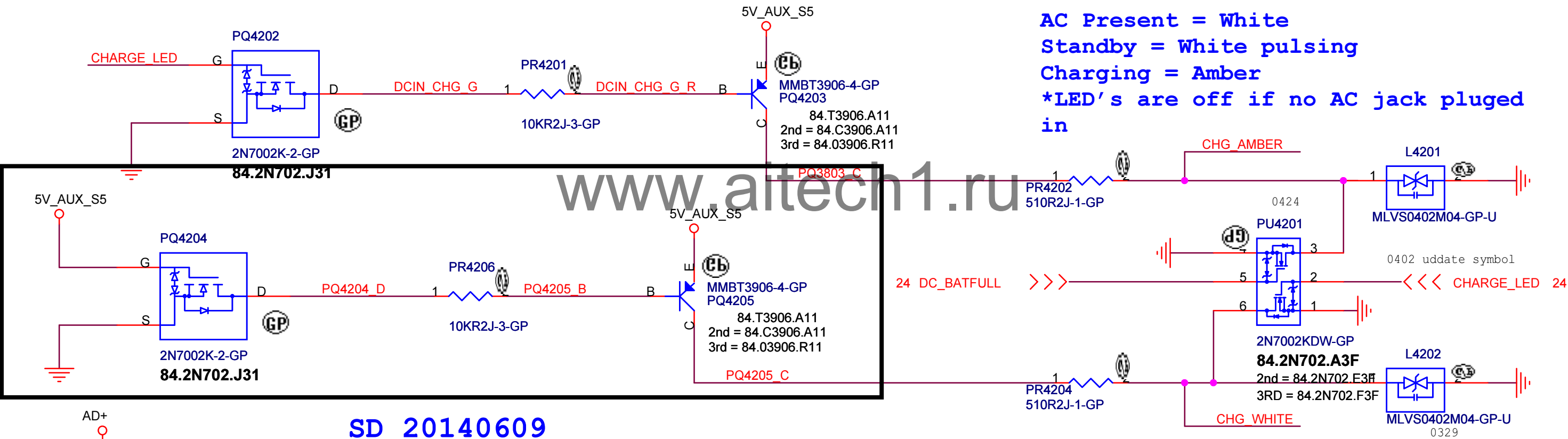
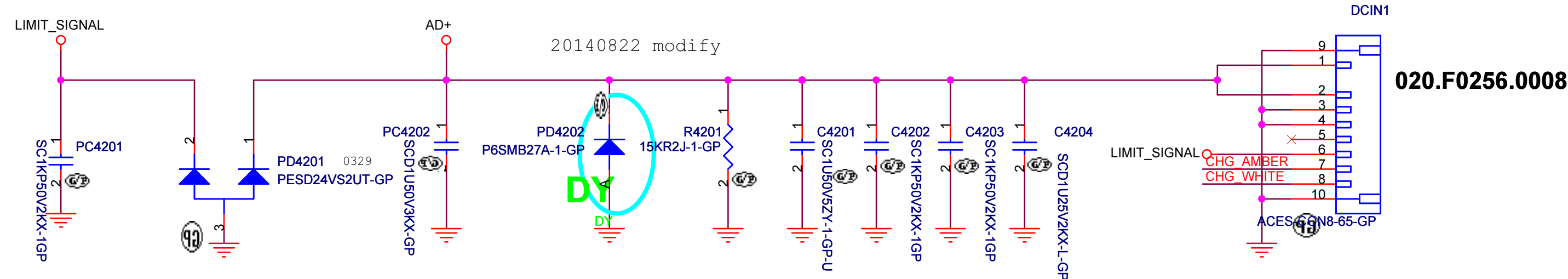
Rev

Fauchon-BDW 13"

SA

Date: Saturday, September 13, 2014

Sheet 41 of 102



20140808 Follow Reacher by Colbert

EV

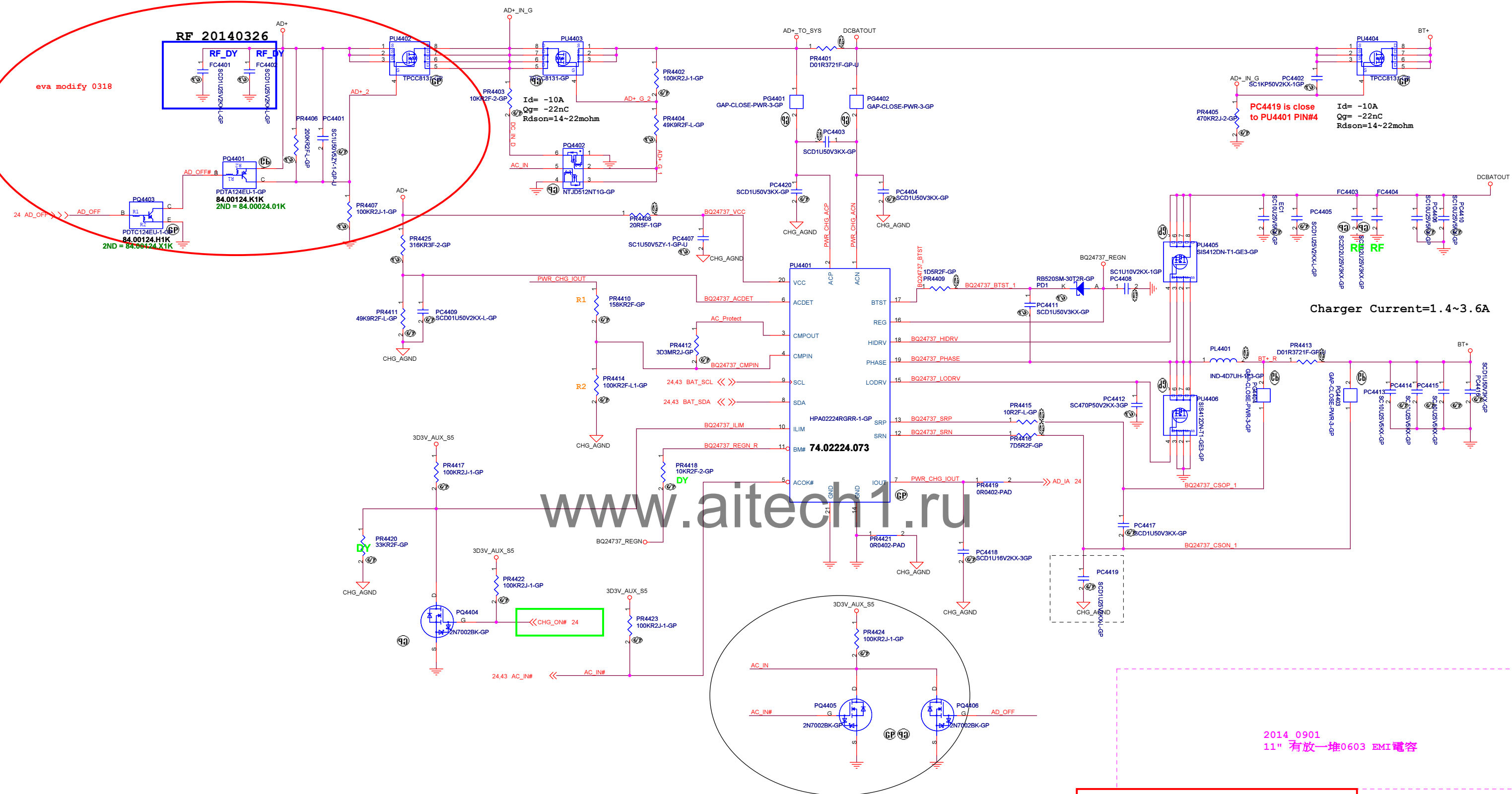
緯創資通 Wistron Corporation
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Title: **DCIN JACK**

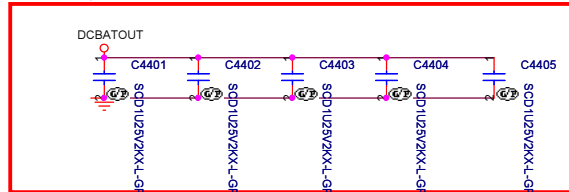
Size A4 Document Number **Fauchon-BDW 13"** Rev **SA**

Date: Wednesday, October 29, 2014 Sheet 42 of 102

SSID = Charger



20140812 Change Charge solution follow Reacher.



SB Add

<Core Design>

Main Func = 3D3V_5V

Design Current=3.3A
4.95A<OCP>5.94A

Design Current=6.85A
10.75A<OCP>12.33A

I/P cap: CHIP CAP C 10U 25V K0805 X5R/ 78.10622.51L
Inductor: CHIP IND 3.3UH PCMC063T-3R3MN Cyntec 28mohm/30mohm Isat =13.5Arms 68.3R310.20A
O/P capCHIP CAP EL 220U 6.3V M6.3*4.4 /Chemi-con/ 18mOhm / 79.22710.3KL
H/S:SIS412 / 24mOhm/30mOhm@4.5Vgs / 84.00412.037
L/S:SIS412 / 24mOhm/30mOhm@4.5Vgs / 84.00412.037

I/P cap: CHIP CAP C 10U 25V K0805 X5R/ 78.10622.51L
Inductor: CHIP CHOKE 2.2U PCMC063T-2R2MN 18mohm/20mohm Isat =14Arms 68.2R210.20B
O/P capCHIP CAP EL 220U 6.3V M6.3*4.4 /Chemi-con/ 18mOhm / 79.22710.3KL
H/S:SIS412 / 24mOhm/30mOhm@4.5Vgs / 84.00412.037
L/S:SIS780 / 14.5mOhm/17.5mOhm@4.5Vgs / 84.00780.037

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title

DCDC-3D3V&5V

Size

A2

Document Number

Fauchon-BDW 13"

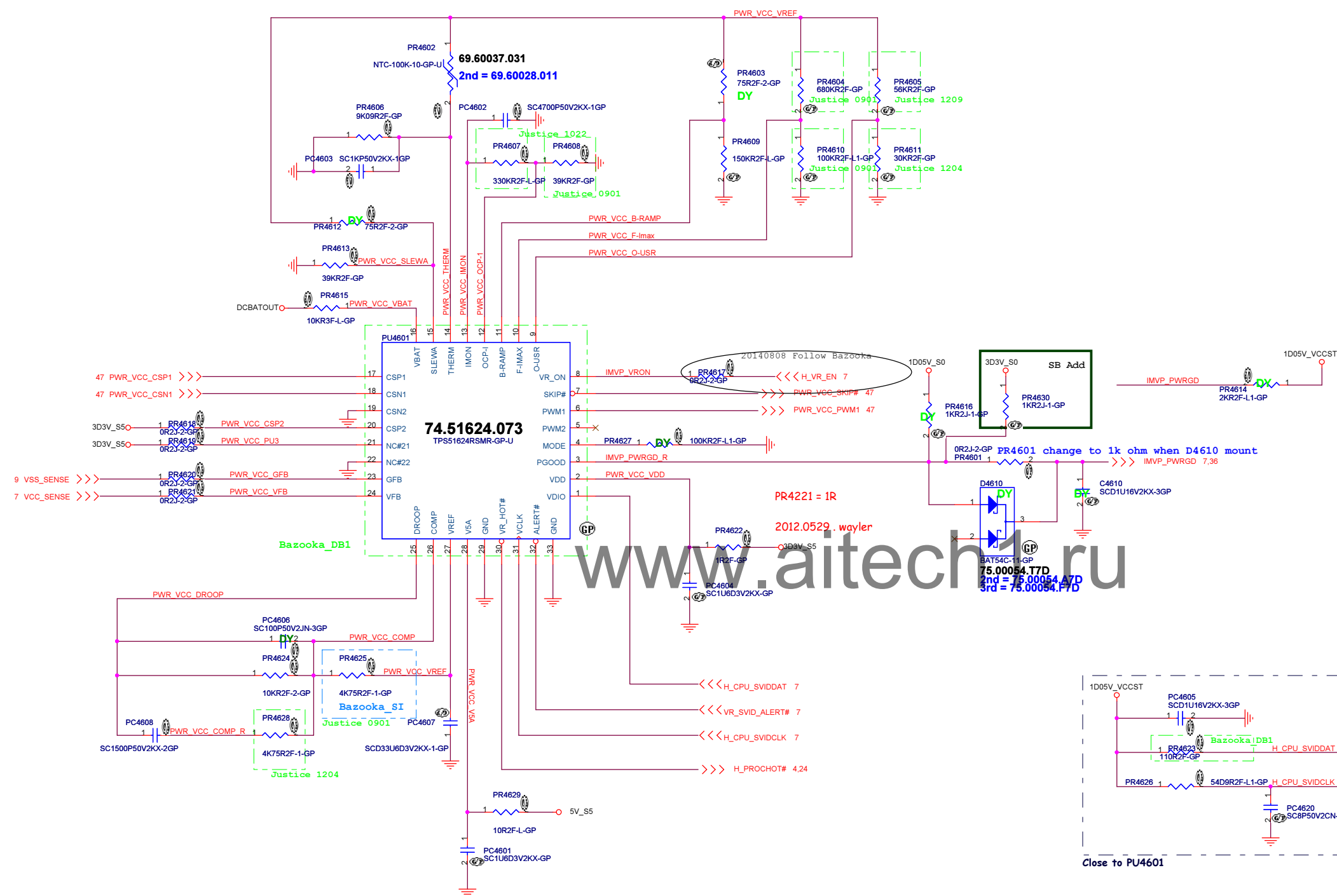
Rev

SA

Date: Monday, October 27, 2014

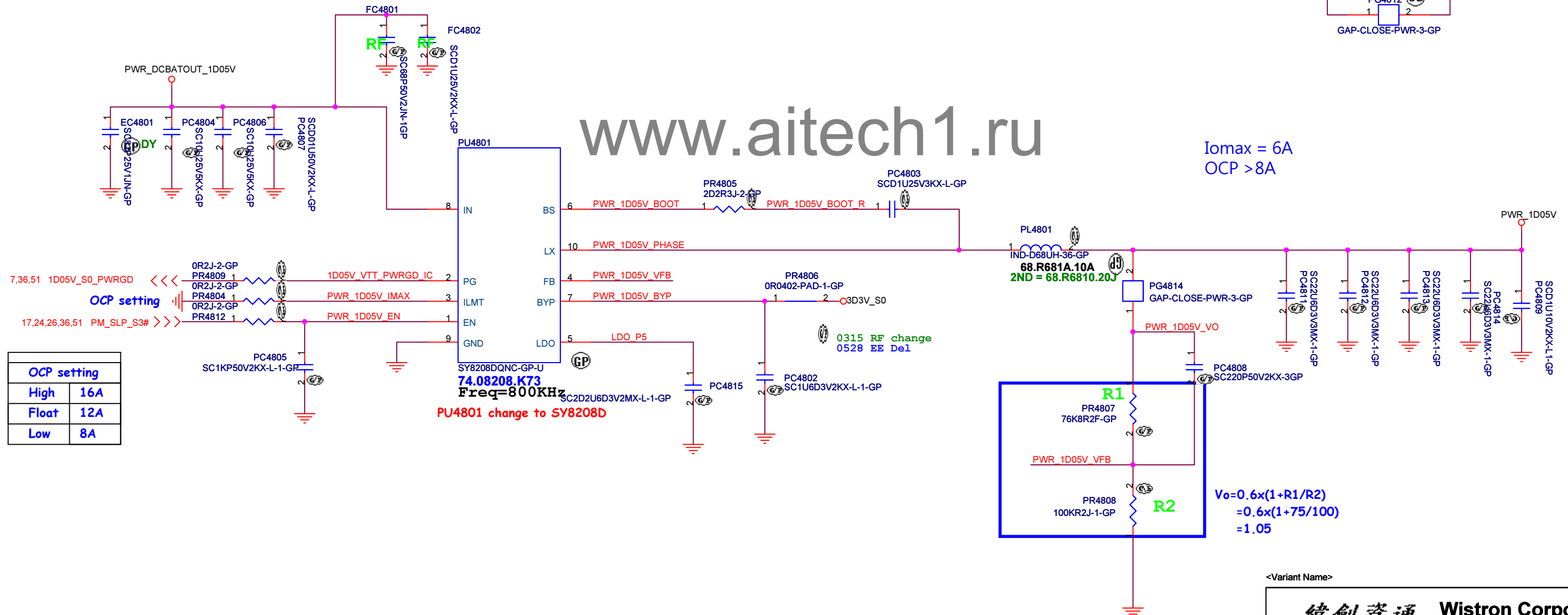
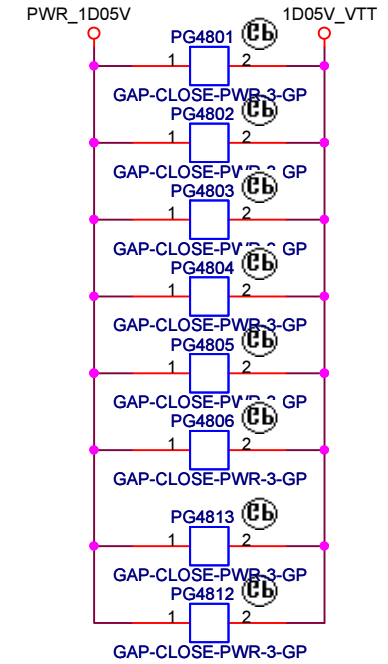
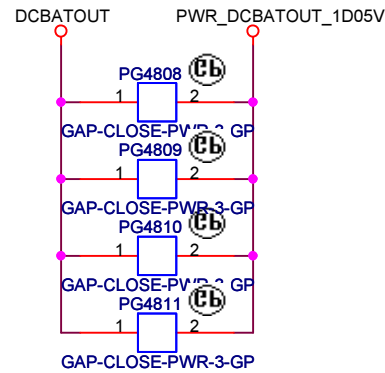
Sheet 45 of 102

SSID = CPU.Regulator




```
SSID = PWR.Plane.Regulator_1p05v
```

SY8208D for 1D05V



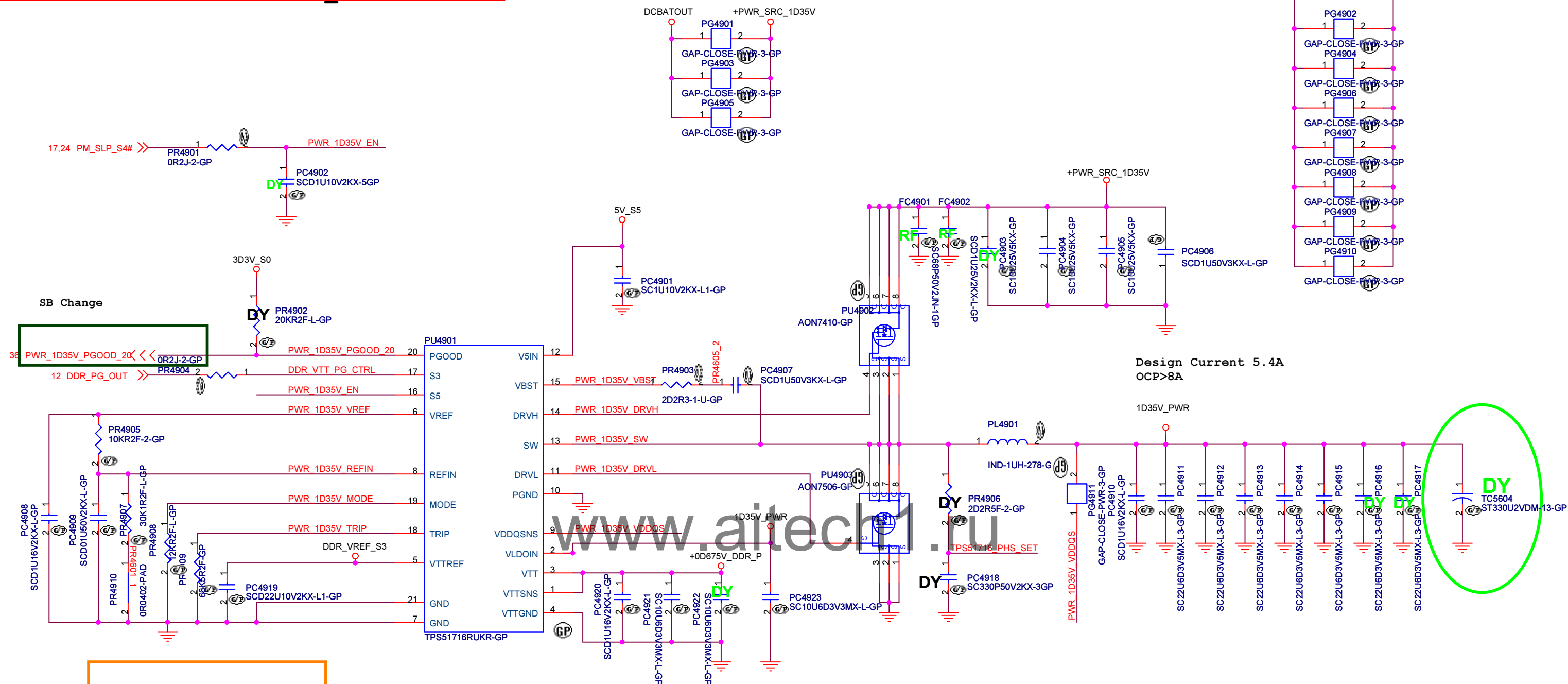
OCP setting	
High	16A
Float	12A
Low	8A

<Variant Name>

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Title			
SY8208D for 1D05V			
Size A3	Document Number Fauchon-BDW 13"		Rev SA
Date:	Monday, October 27, 2014	Sheet 48 of	102

SSID = PWR.Plane.Regulator 1p35v0p675v



S3/S5 Power State Control

STATE	S3	S5	VREF	VDDQ	VTTREF	VTT
S0	HI	HI	ON	ON	ON	ON
S3	LO	HI	ON	ON	ON	OFF(High-Z)
S4/S5	LO	LO	OFF	OFF(Discharge)	OFF(Discharge)	OFF(Discharge)

MODE Selection

MODE NO.	RESISTANCE BETWEEN MODE AND GND (kΩ)	CONTROL MODE	SWITCHING FREQUENCY (kHz)	DISCHARGE MODE
3	33	D-CAP2	500	Non-Tracking
2	22		670	
1	12		670	Tracking
0	1		500	

<Core Design>

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Title			
TPS51716(VDDQ_VTT)			
Size A3	Document Number		Rev
	Fauchon-BDW 13"		SA
Date:	Monday, October 27, 2014	Sheet 49 of	102

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<Core Design>

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Title

(Reserved)1D8V_S0

SizeA3

Document Number

RevSA

Date: Saturday, September 13, 2014

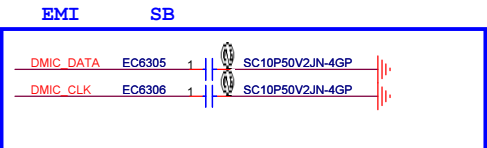
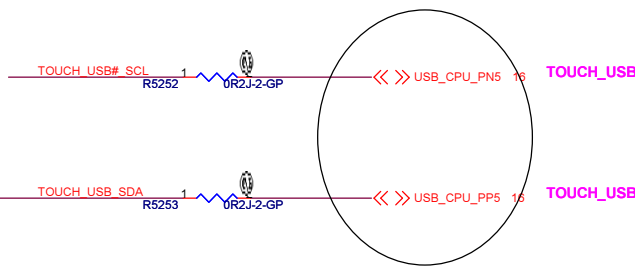
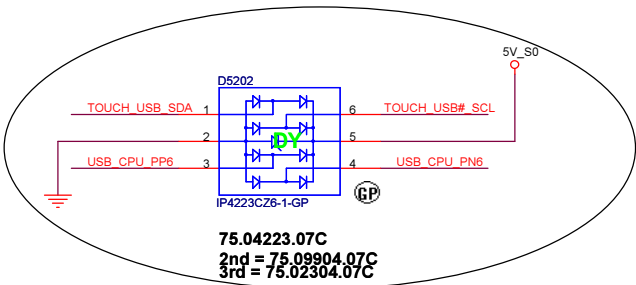
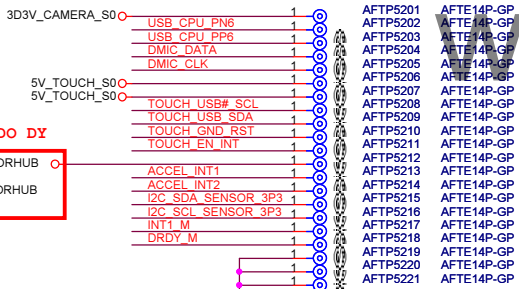
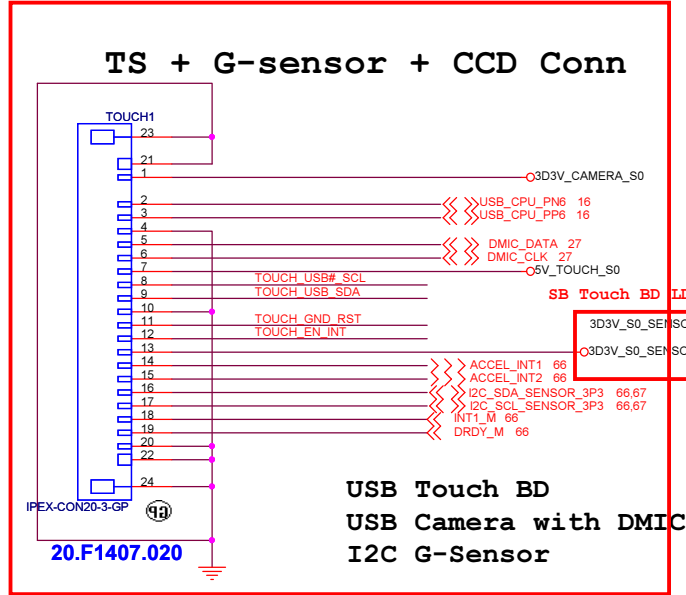
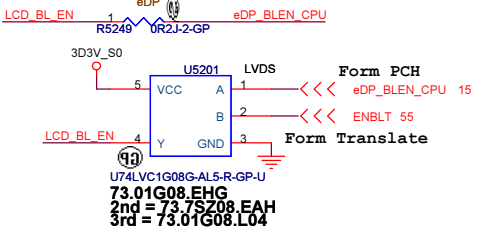
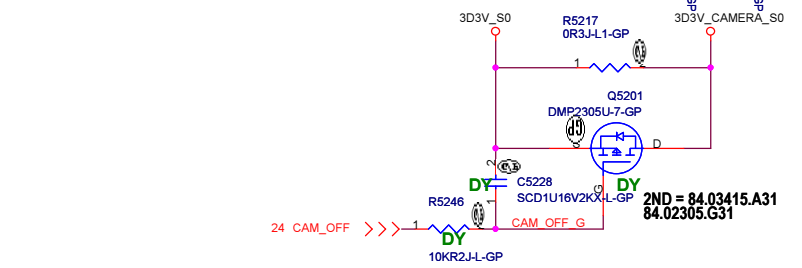
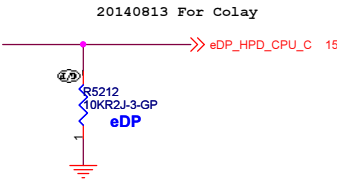
Sheet 50 of 102

Title

Size

Rev

Sheet	51	of	102
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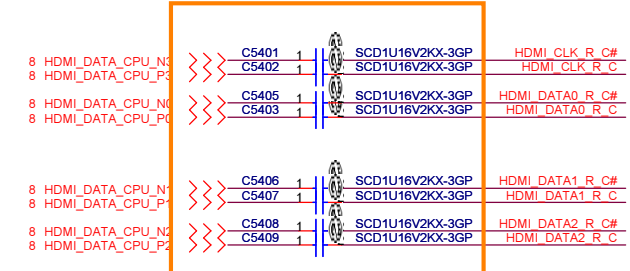
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Taipei Hsien 221, Taiwan, R.O.C.

Title
CRT Board Connector

Size A3	Document Number Fauchon-BDW 13"	Rev SA
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Date: Saturday, September 13, 2014 Sheet 53 of 102

HDMI Connector

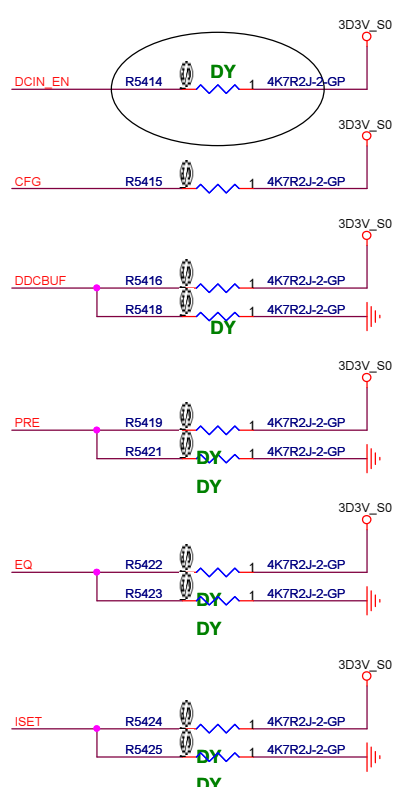


Close to HDMI U5401

Need check 1.5V power regulator
CAP palace near IC

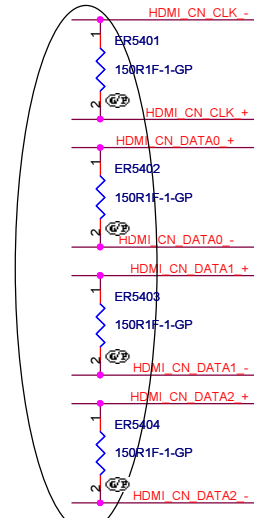
all cap close to IC

NEED CONFIRM SETTING

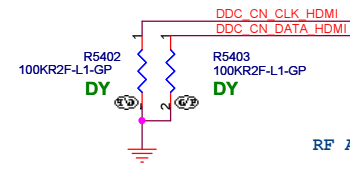


2013.07.24 EE change

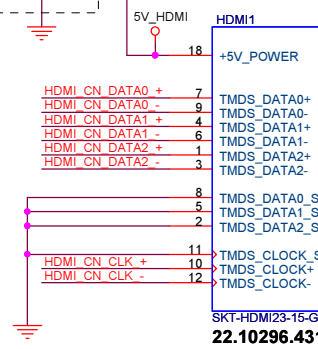
20140806



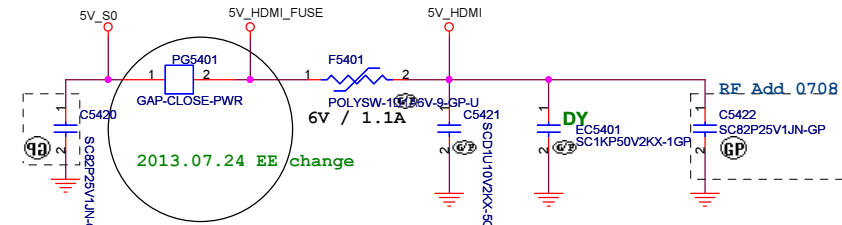
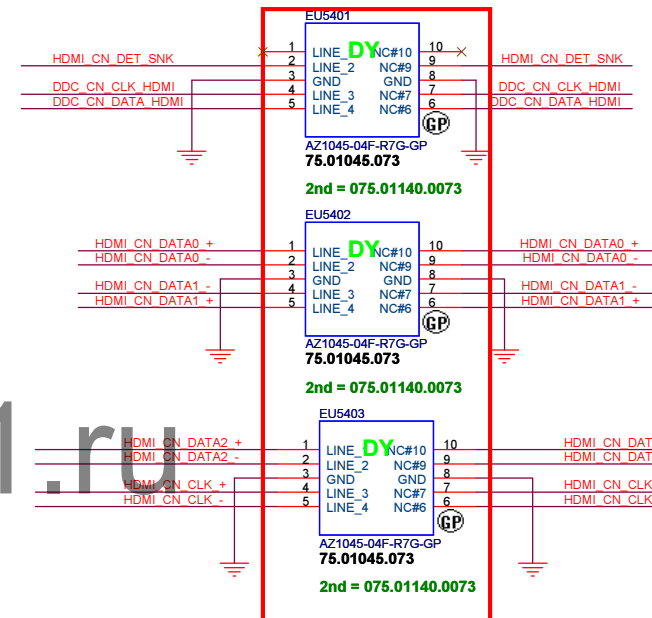
SB EMI change to 150ohm ,mount



RF Add 0708



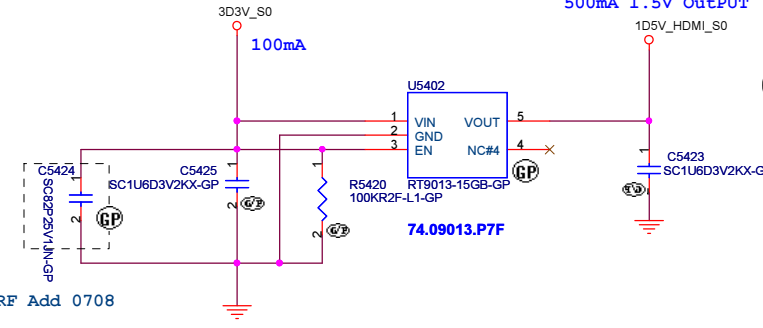
SB Change
83.00056.Q11



2013.07.24 EE change

RF Add 0708

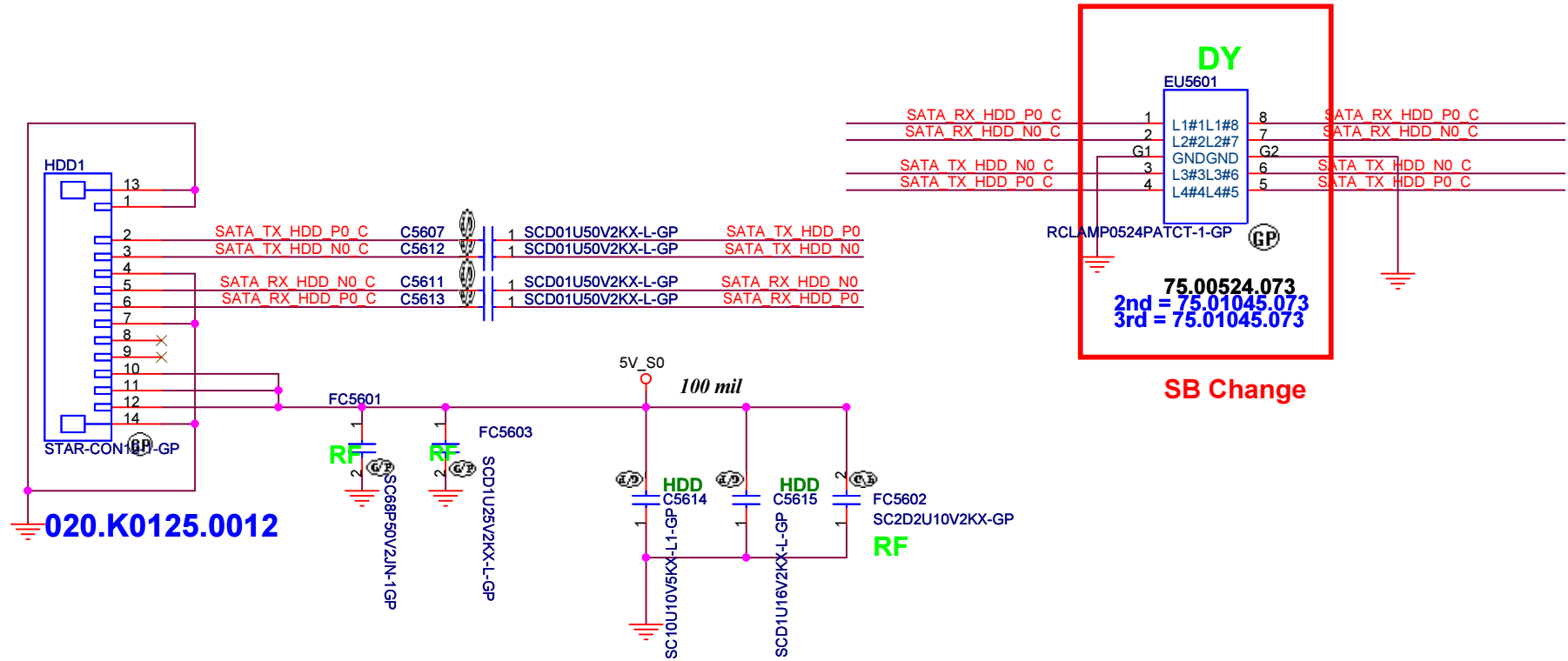
500mA 1.5V OutPUT



RF Add 0708

SSID = SATA

SATA HDD Connector



SATA redriver Co-lay

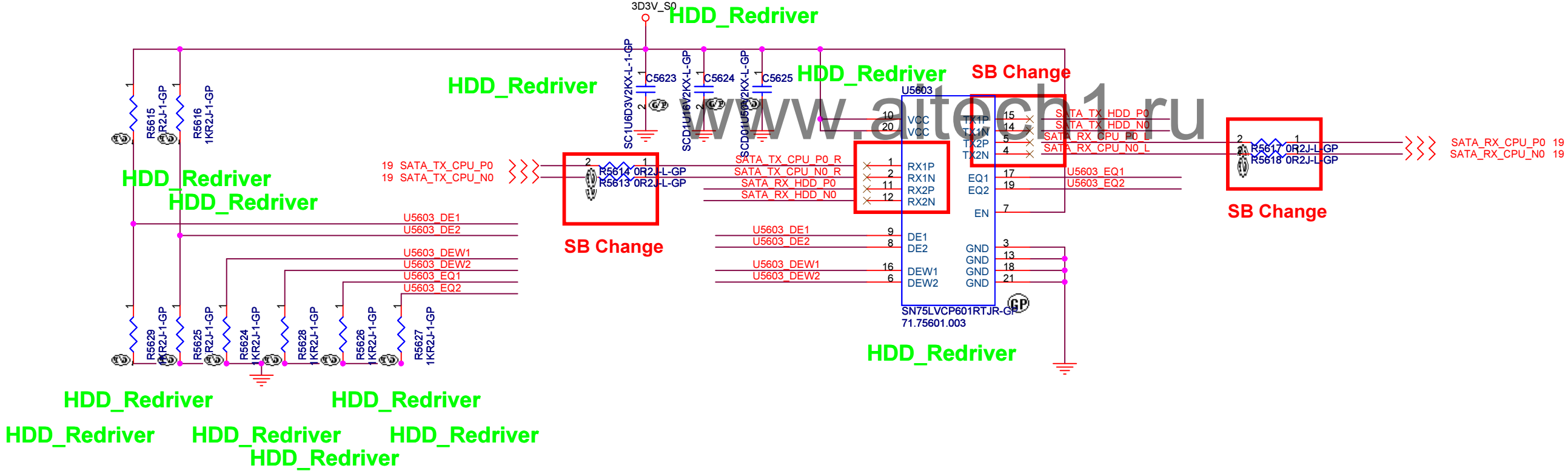
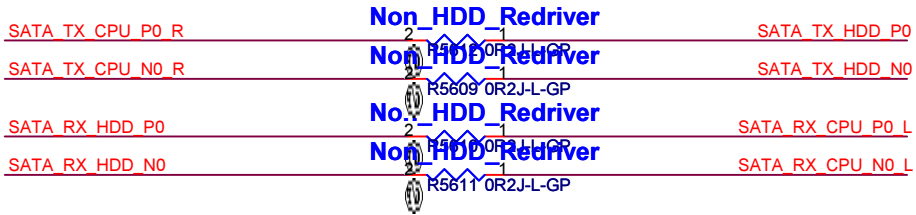
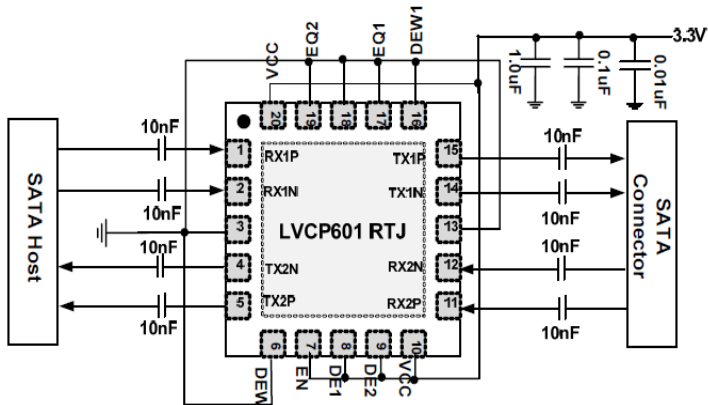


Figure 5: Typical Device Implementation



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E-SATA

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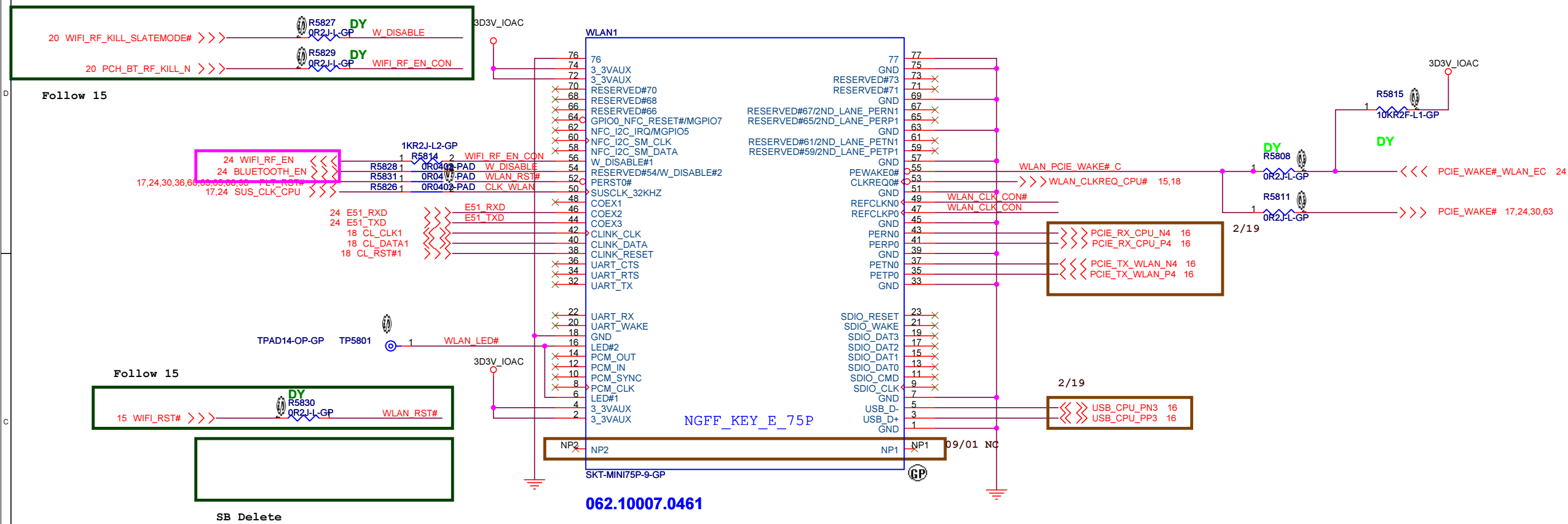
Sheet

57

of

102

SSID = Wireless Mini Card Connector(802.11a/b/g/n)



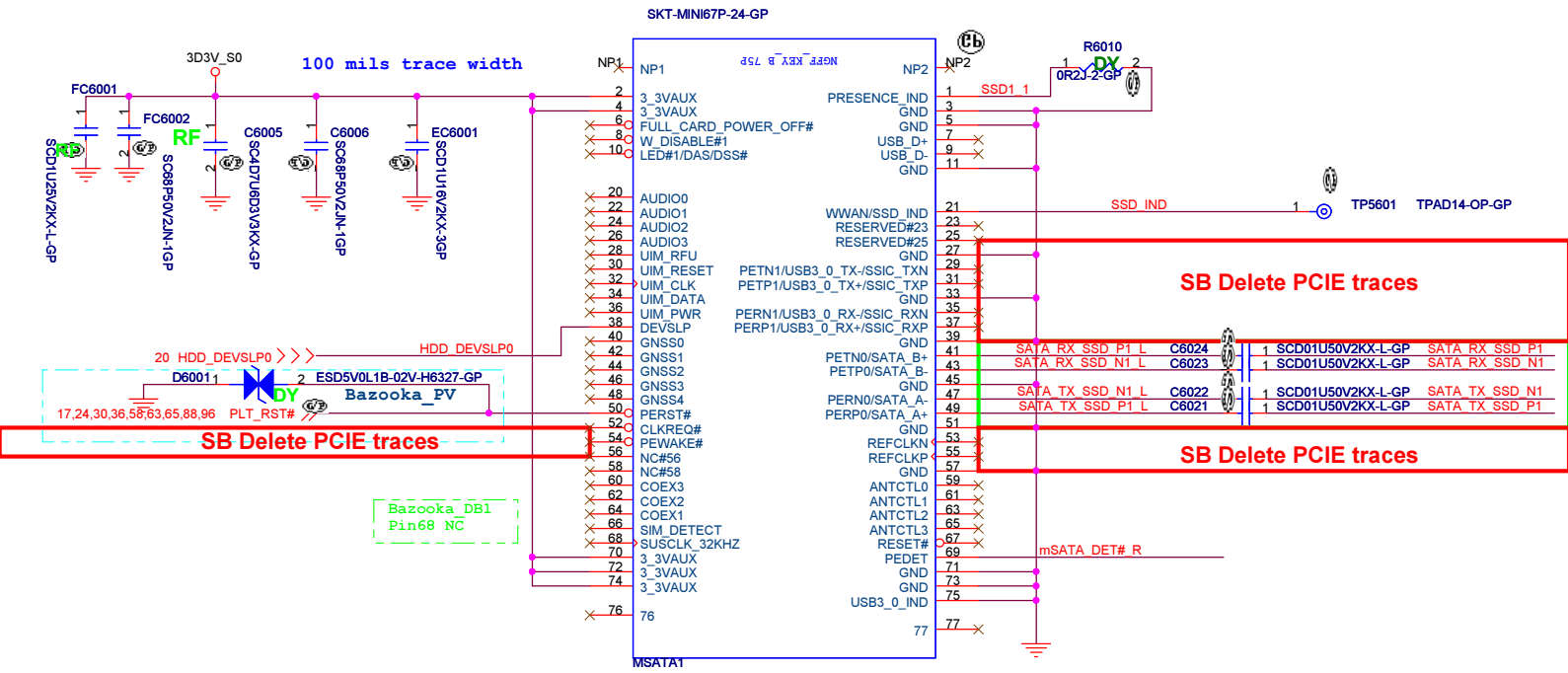


20140805
Remove the WWAN function(11" Only)

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SSID = SATA SSD

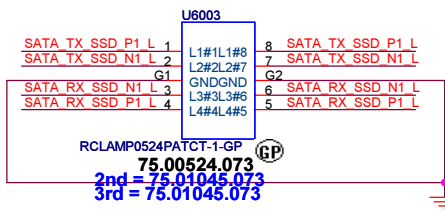
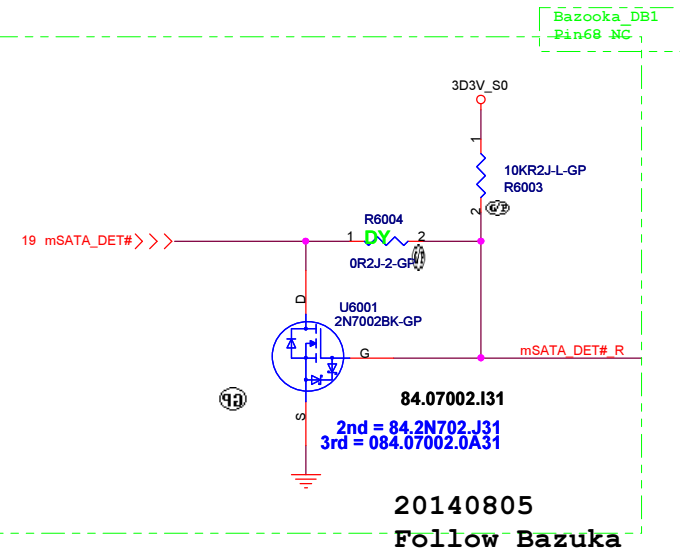
SSD slot C key B



20140912

NGFF

062.10007.0451



SATA redriver Co-lay

SB Change to Bypass only

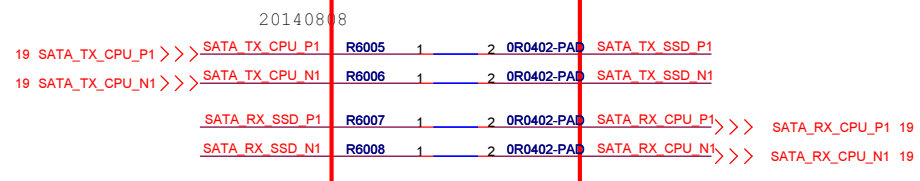
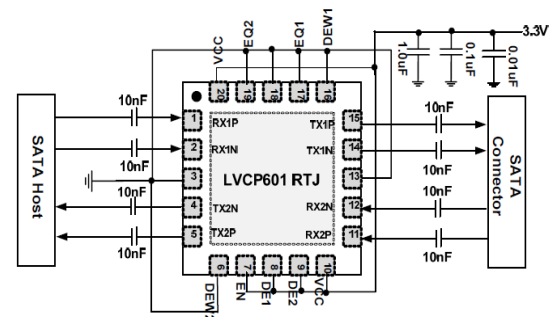


Figure 5: Typical Device Implementation



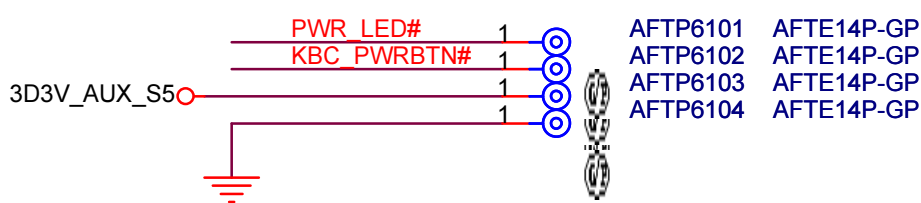
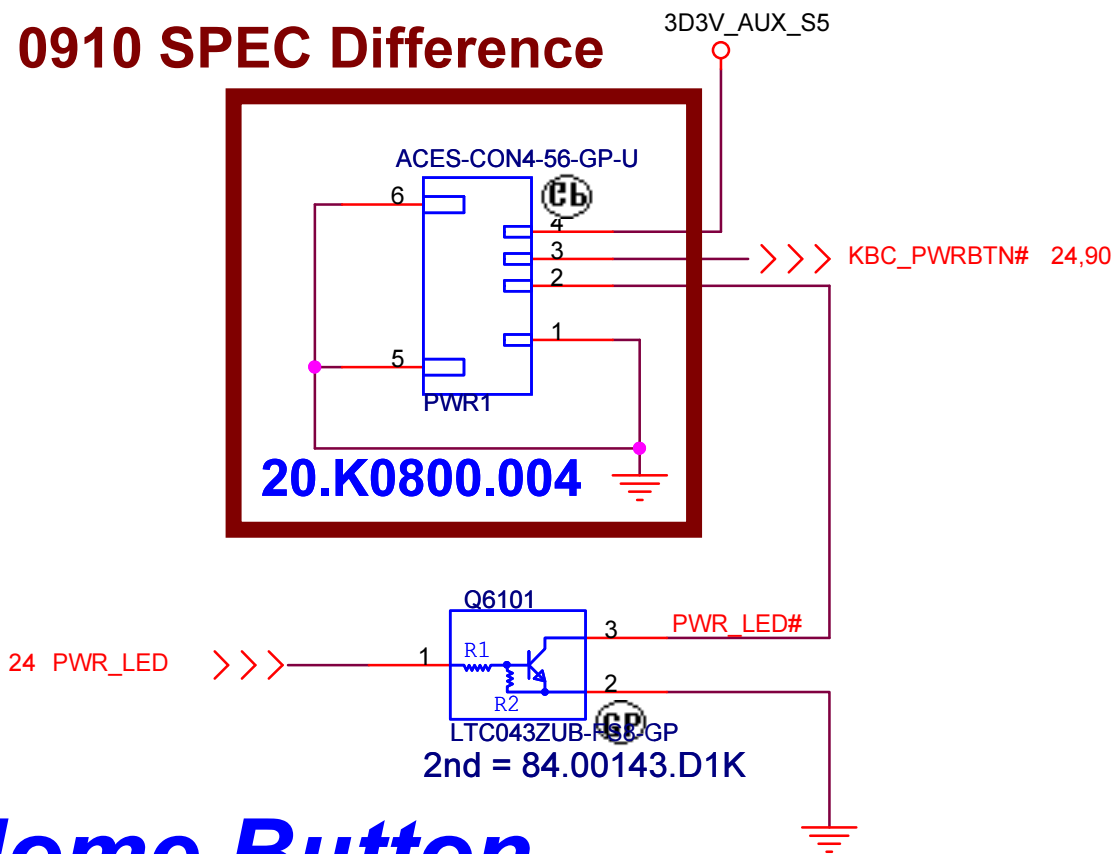
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Title		
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Size	Document Number	Rev
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Date:	Monday, October 27, 2014	Sheet 60 of 102

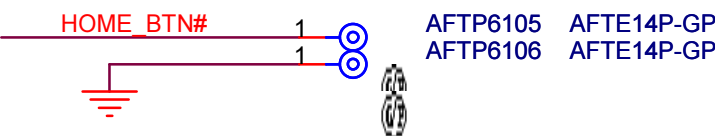
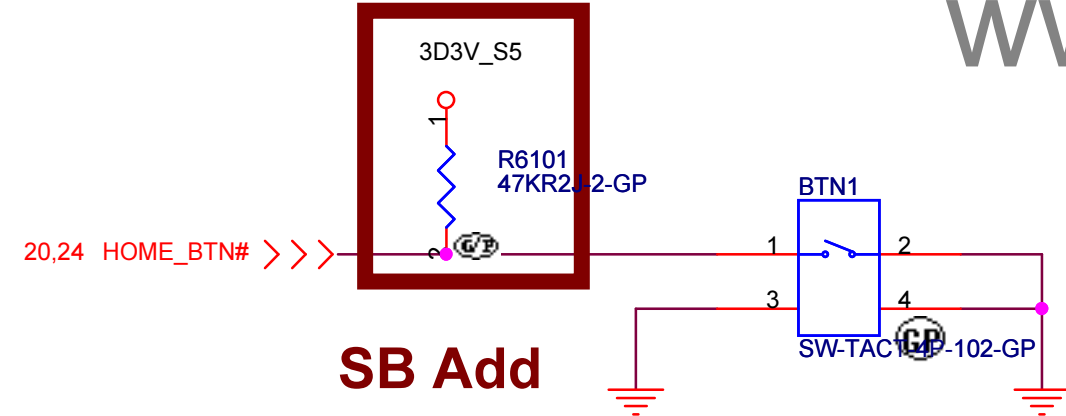
Power Button

0910 SPEC Difference



AFTP6101	AFTE14P-GP
AFTP6102	AFTE14P-GP
AFTP6103	AFTE14P-GP
AFTP6104	AFTE14P-GP

Home Button



AFTP6105	AFTE14P-GP
AFTP6106	AFTE14P-GP

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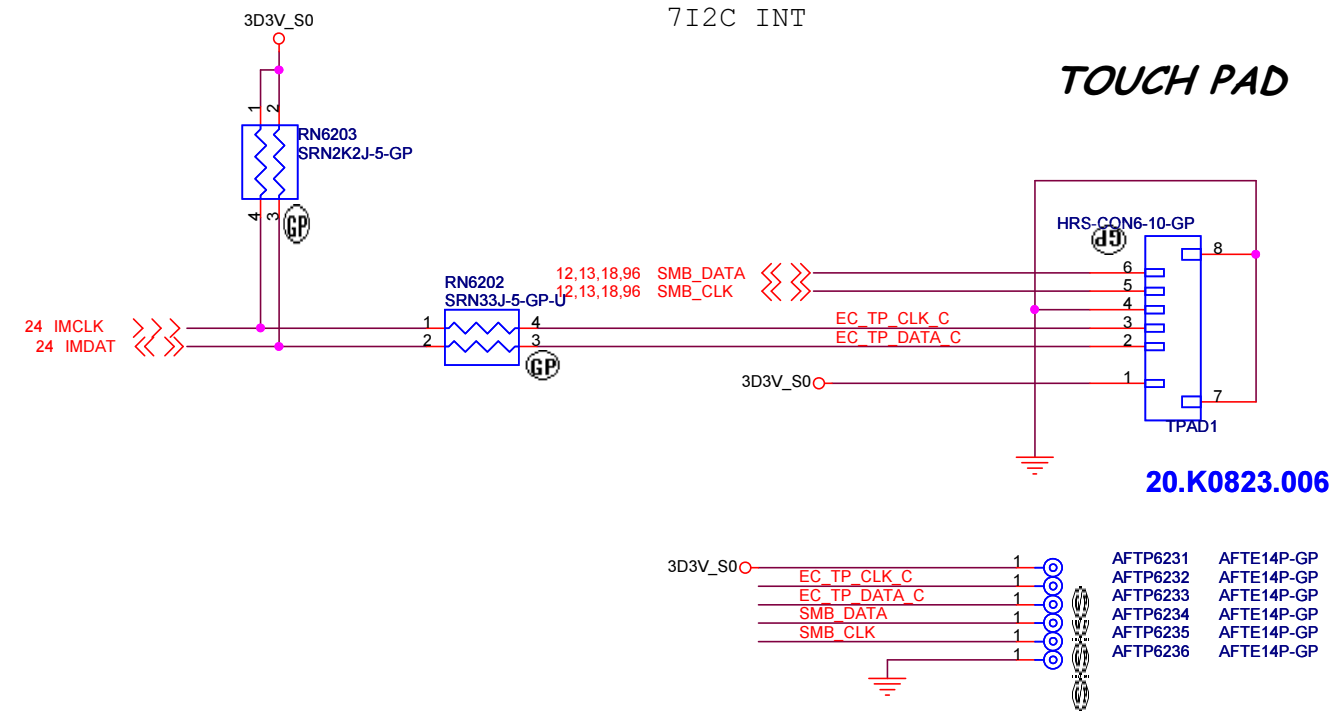
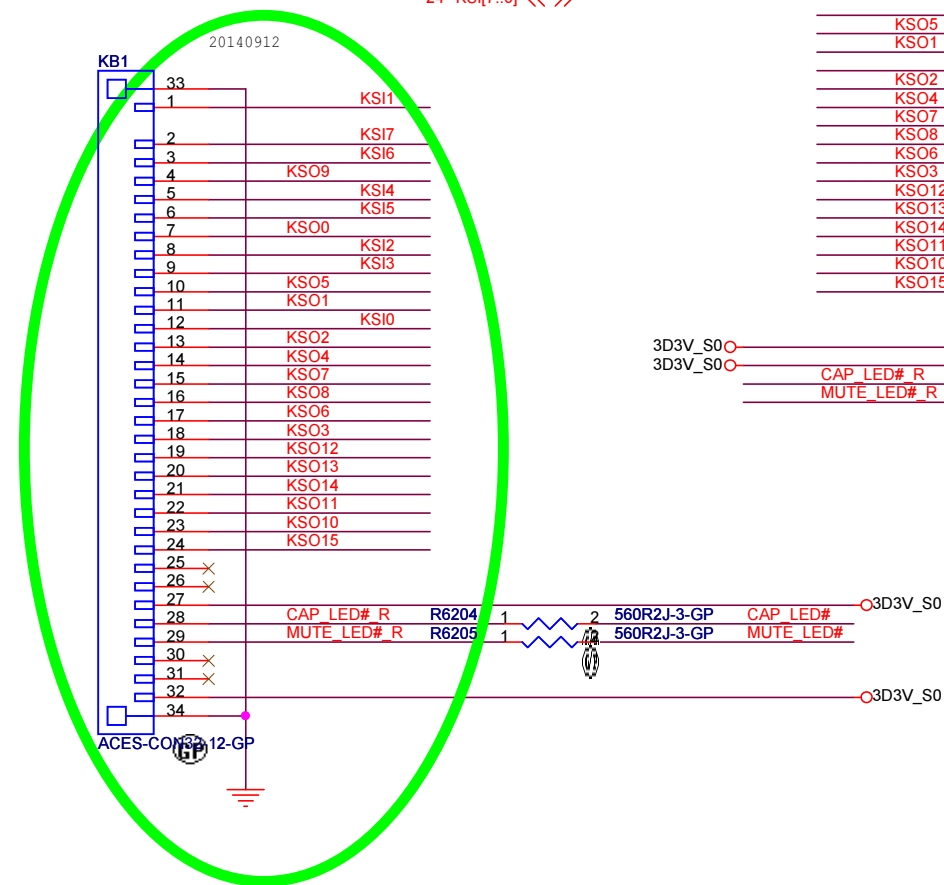
SB Add

EV

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Title			
LED Bard/Power Button			
Size	Document Number		Rev
A4	Fauchon-BDW 13"		SA
Date:	Monday, November 03, 2014		Sheet 61 of 102

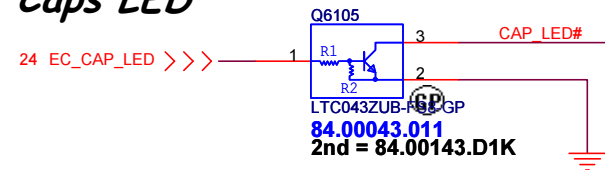
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020.K0116.0032

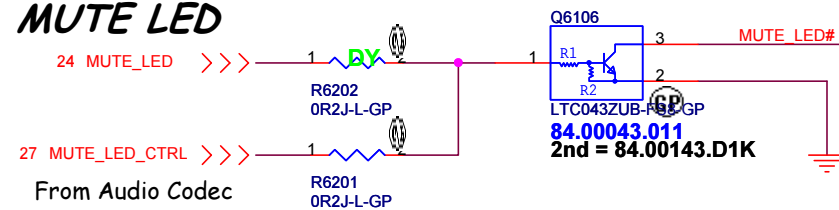


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Caps LED



MUTE LED



<Variant Name>

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Title

Touch Pad

Size
Custom

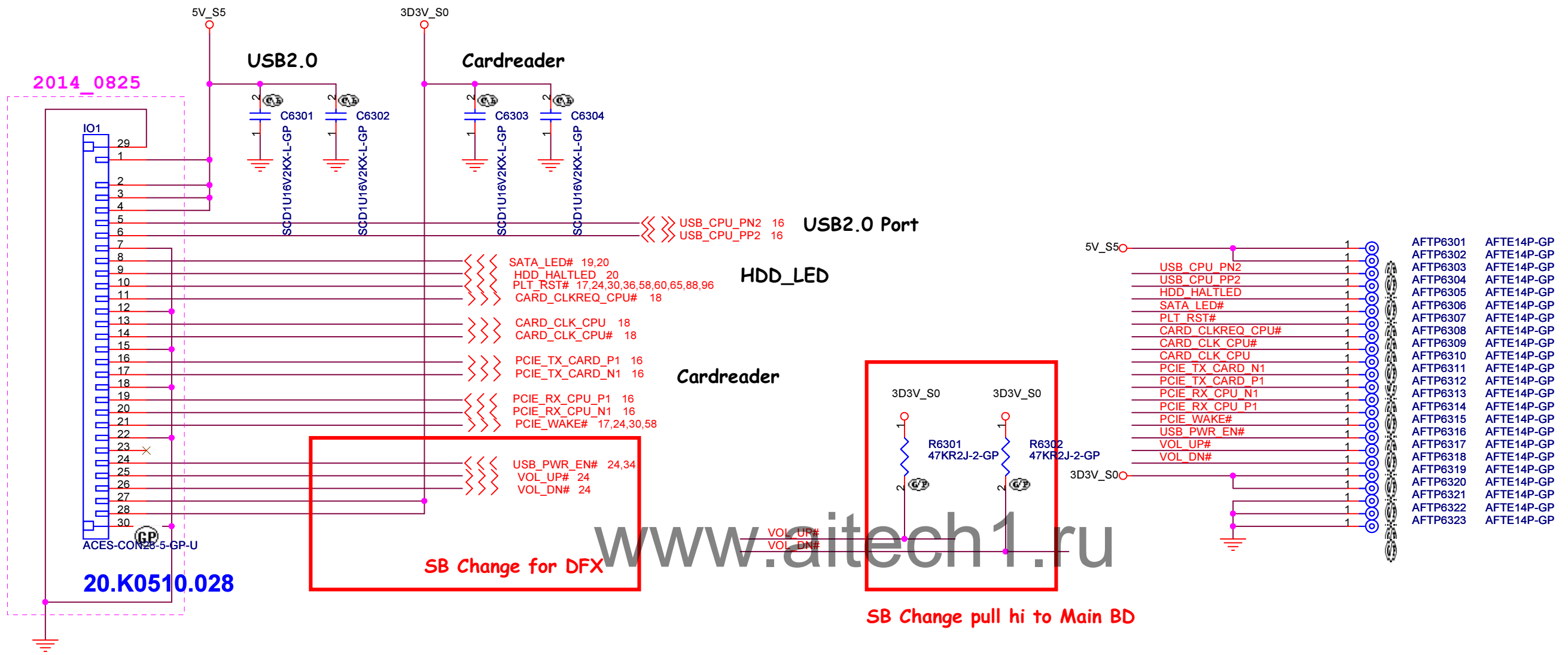
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Sheet 62 of 102



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Title

IO Board Connector

Size Custom

Document Number

Fauchon-BDW 13"

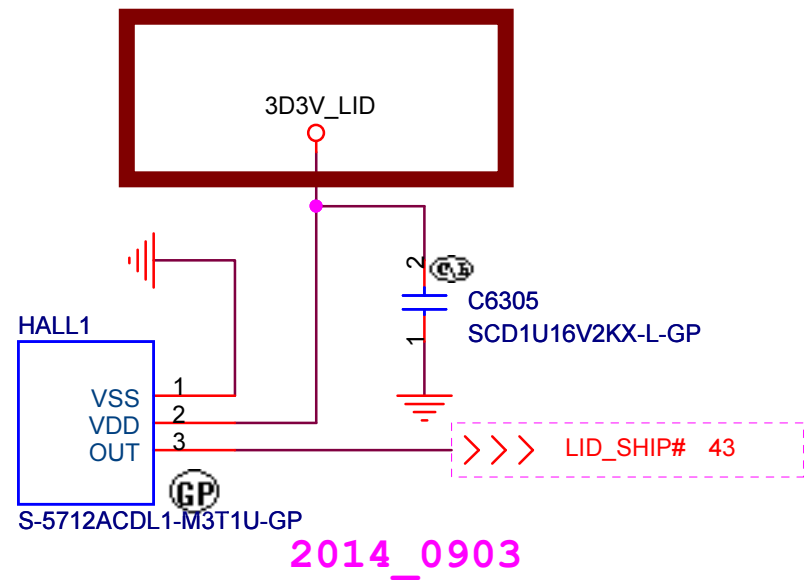
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Sheet 63 of 102

0910 Change power



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<div>Hall Sensor</div>			
Size A4	Document Number <div>Fauchon-BDW 13"</div>		Rev <div>SA</div>
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ACCELEROMETER

To KBC
for HDD Protect

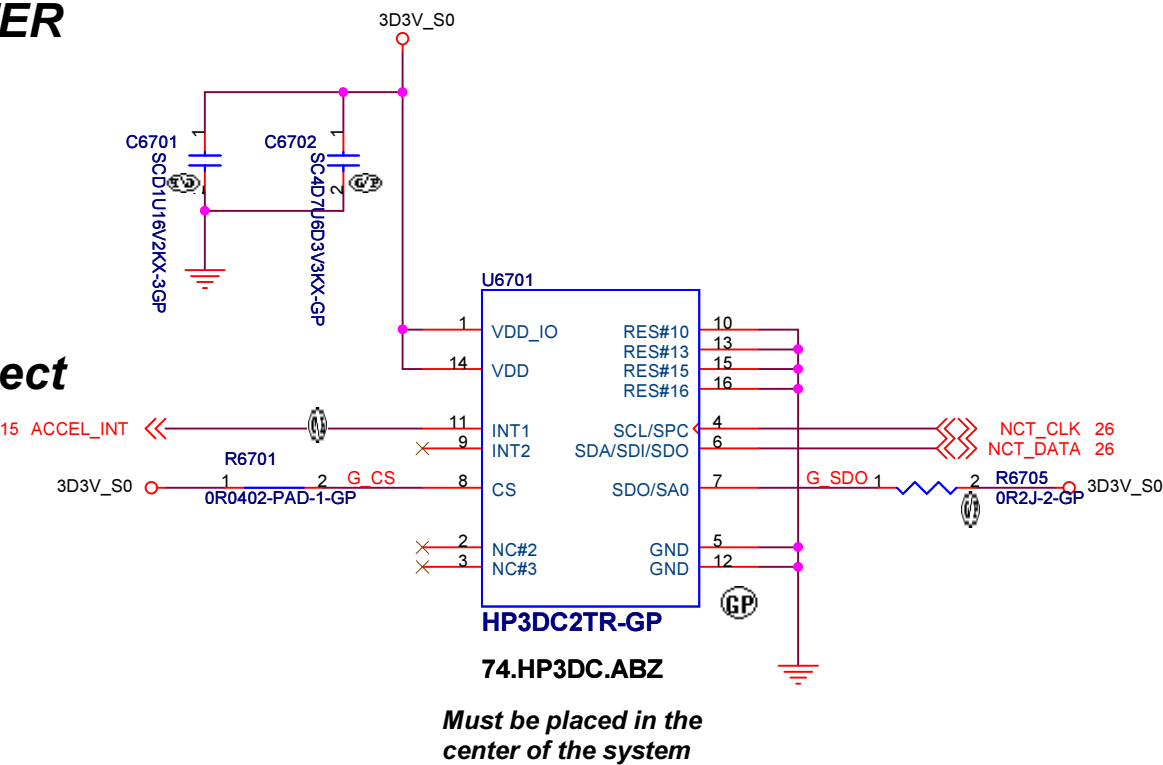


Table 10. SAD+Read/Write patterns

Command	SAD[6:1]	SAD[0] = SA0	R/W	SAD+R/W
Read	010100	0	1	01010001 (51h)
Write	010100	0	0	01010000 (50h)
Read	010100	1	1	01010011 (53h)
Write	010100	1	0	01010010 (52h)

To Sensor HUB
for LCD angle

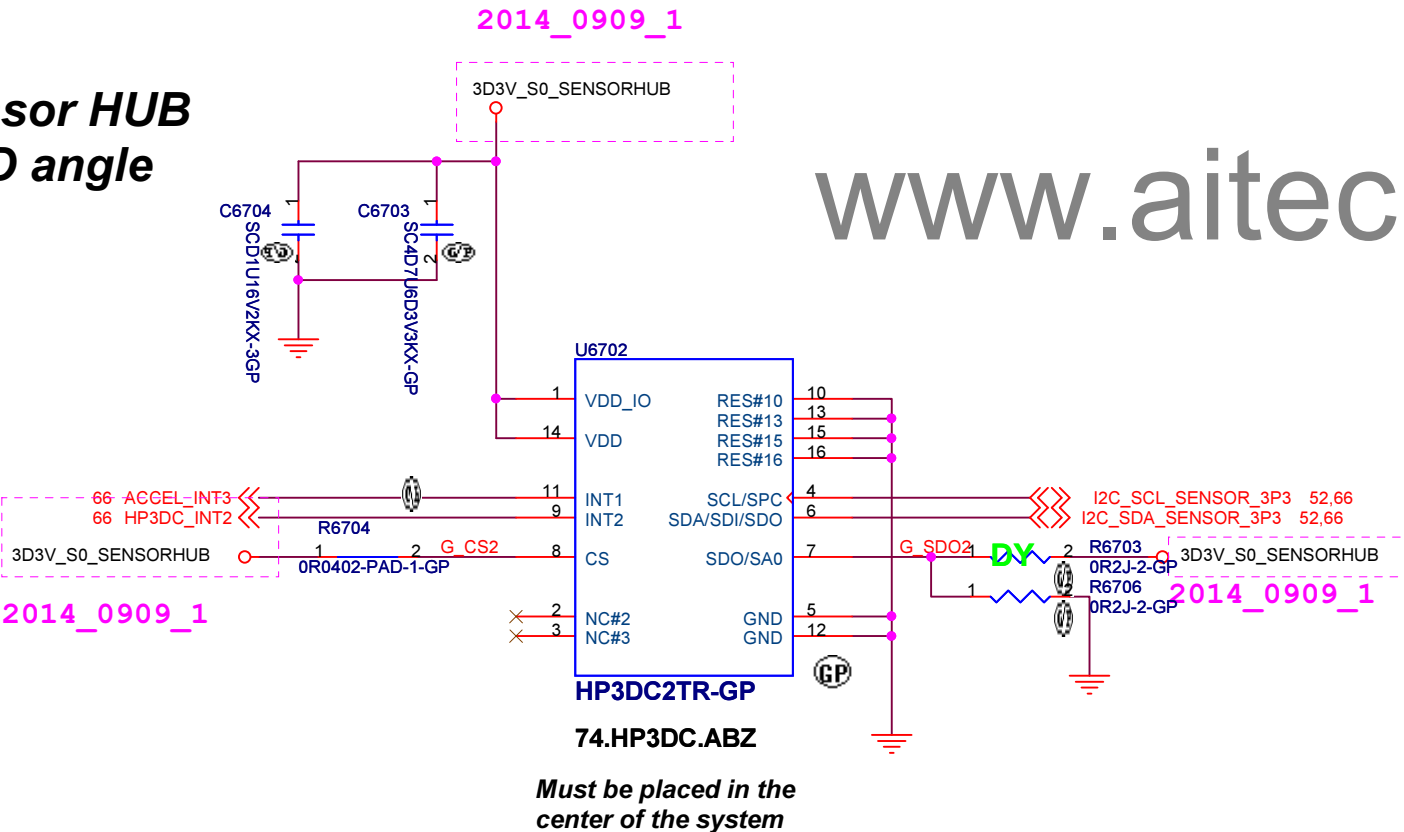


Table 10. SAD+Read/Write patterns


Command	SAD[6:1]	SAD[0] = SA0	R/W	SAD+R/W
Read	010100	0	1	01010001 (51h)
Write	010100	0	0	01010000 (50h)
Read	010100	1	1	01010011 (53h)
Write	010100	1	0	01010010 (52h)

ULT

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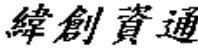
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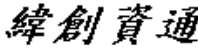
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Custom	Fauchon-BDW 13"		SA
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Sheet 72 of 102

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GPU_Digitalout			
Size	Project Name		Rev
	MYBO AMD		SA
Date:	Saturday, September 13, 2014	Sheet 74 of	102

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AMD Bemma

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Date: Saturday, September 13, 2014		Sheet 75	of 102

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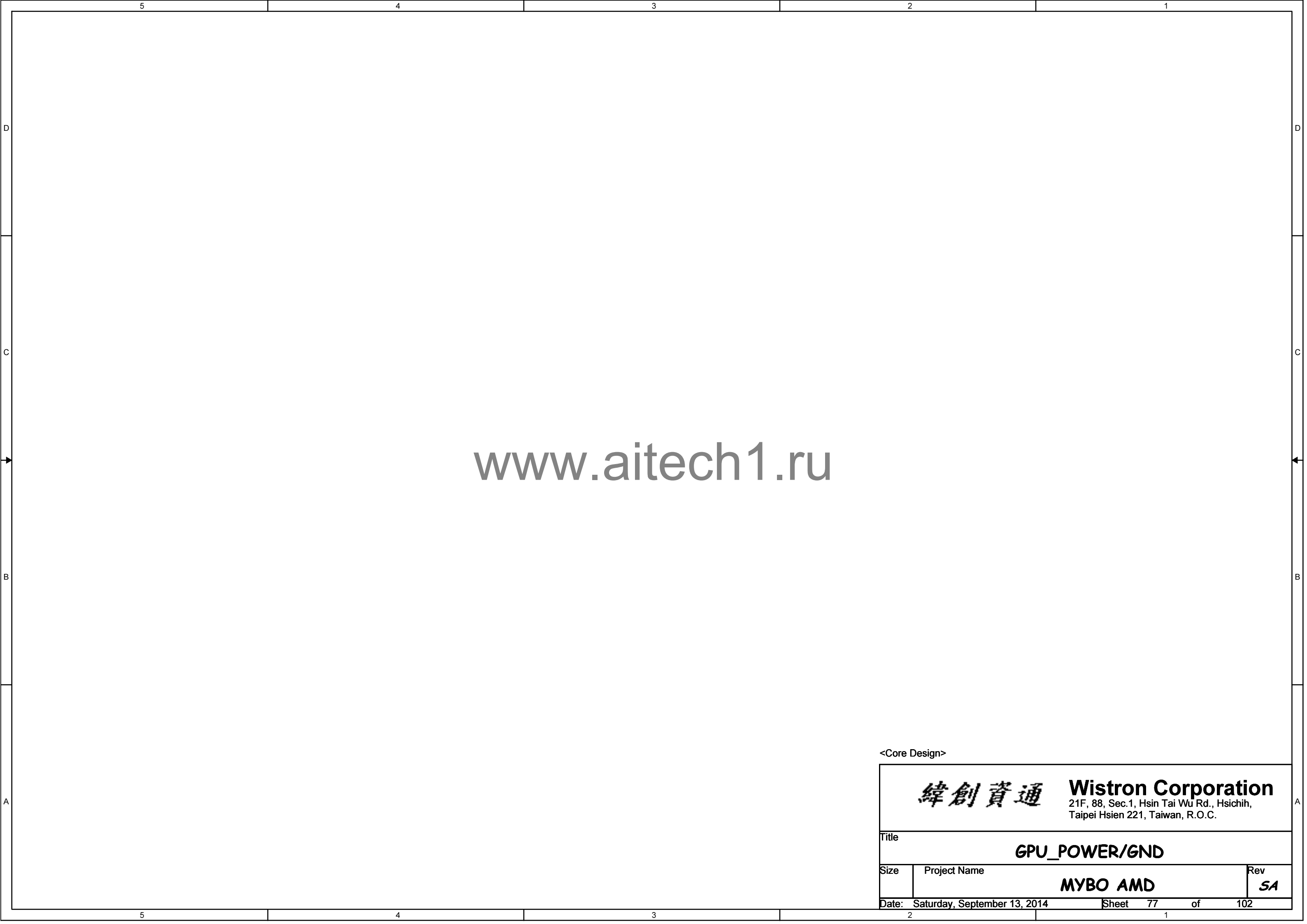
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GPU_GPIO/STRAP


SizeProject NameRev

MYBO AMDSA

Date: Saturday, September 13, 2014Sheet 76 of 102



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Date:	Saturday, September 13, 2014	Sheet 77 of	102

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A3	Fauchon-BDW 13"
Date:	Rev
Saturday, September 13, 2014	SA
Sheet	78 of 102

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Document Number

Rev
SA

Date: Saturday, September 13, 2014

Sheet 79 of 102

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VGA 1D8V/ 0D95V	
Size	Document Number
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Date:	Saturday, September 13, 2014
Sheet	82 of 102

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Sheet 83 of 102

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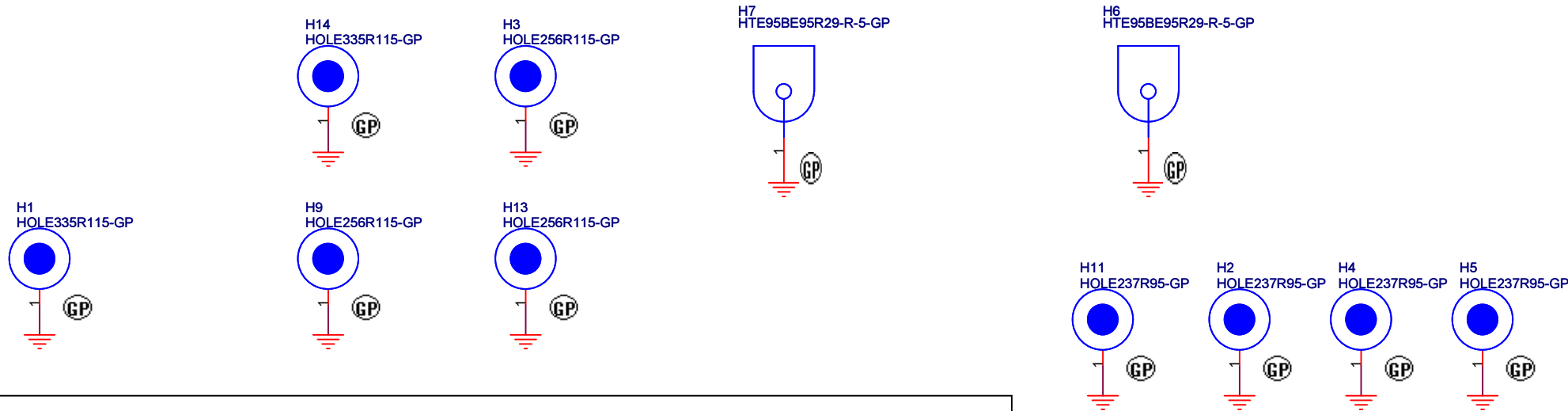
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DISCRETE VGA POWER	
Size	Document Number
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Date:	Rev
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Sheet	84 of 102

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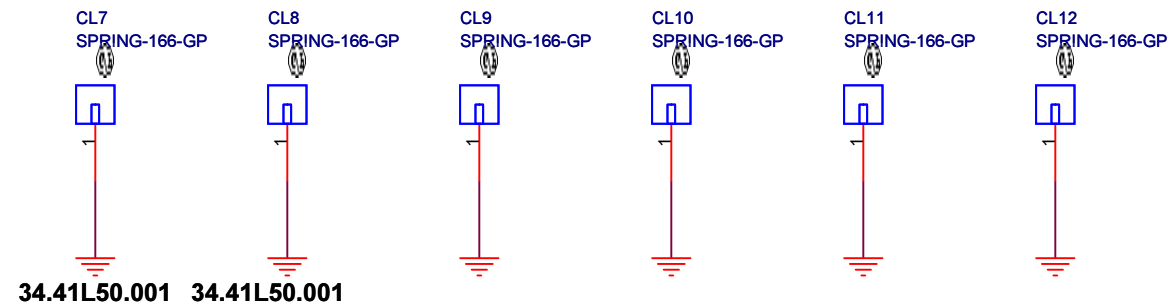
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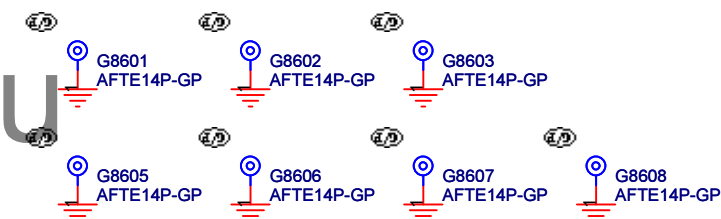
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Title		
Switchable GFX LCD(2/2)		
Size	Document Number	Rev
A4	Fauchon-BDW 13"	SA
Date:	Saturday, September 13, 2014	Sheet 85 of 102



for DDR SO-DIMM 34.41L50.001 34.41L50.001 34.41L50.001 34.41L50.001



GND PAD

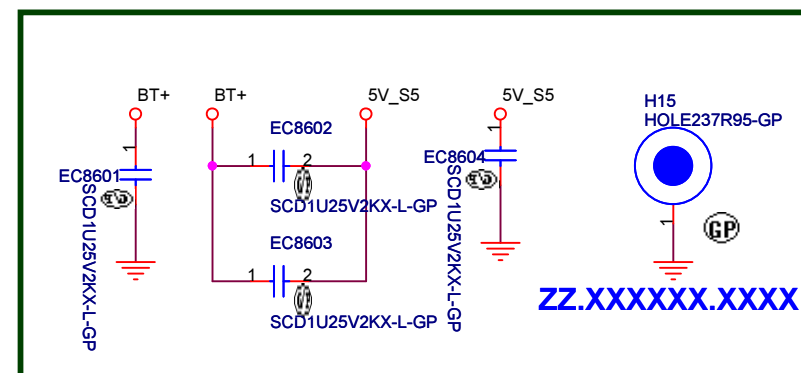


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for USB3.0

34.41L50.001

34.41L50.001



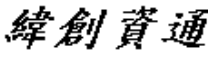
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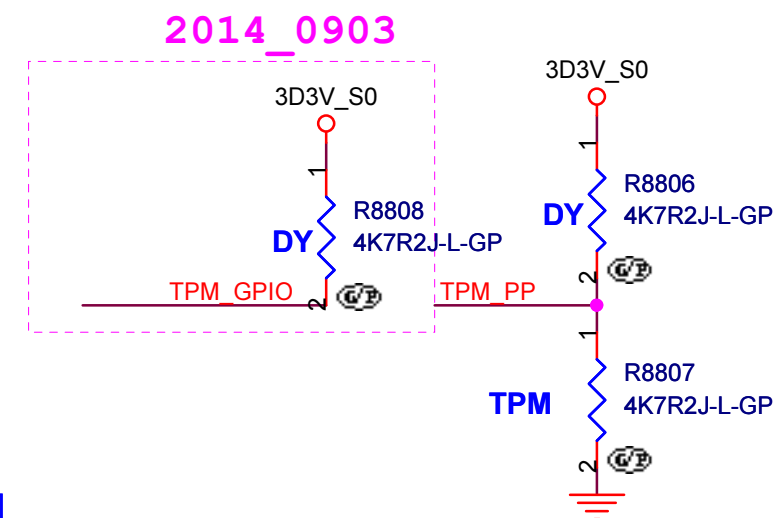
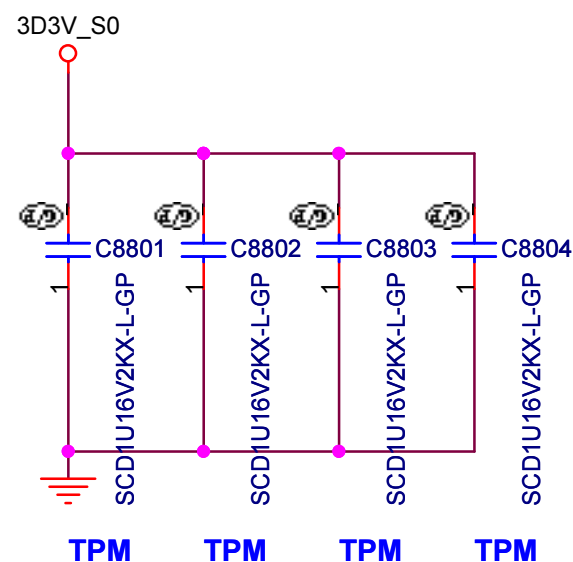
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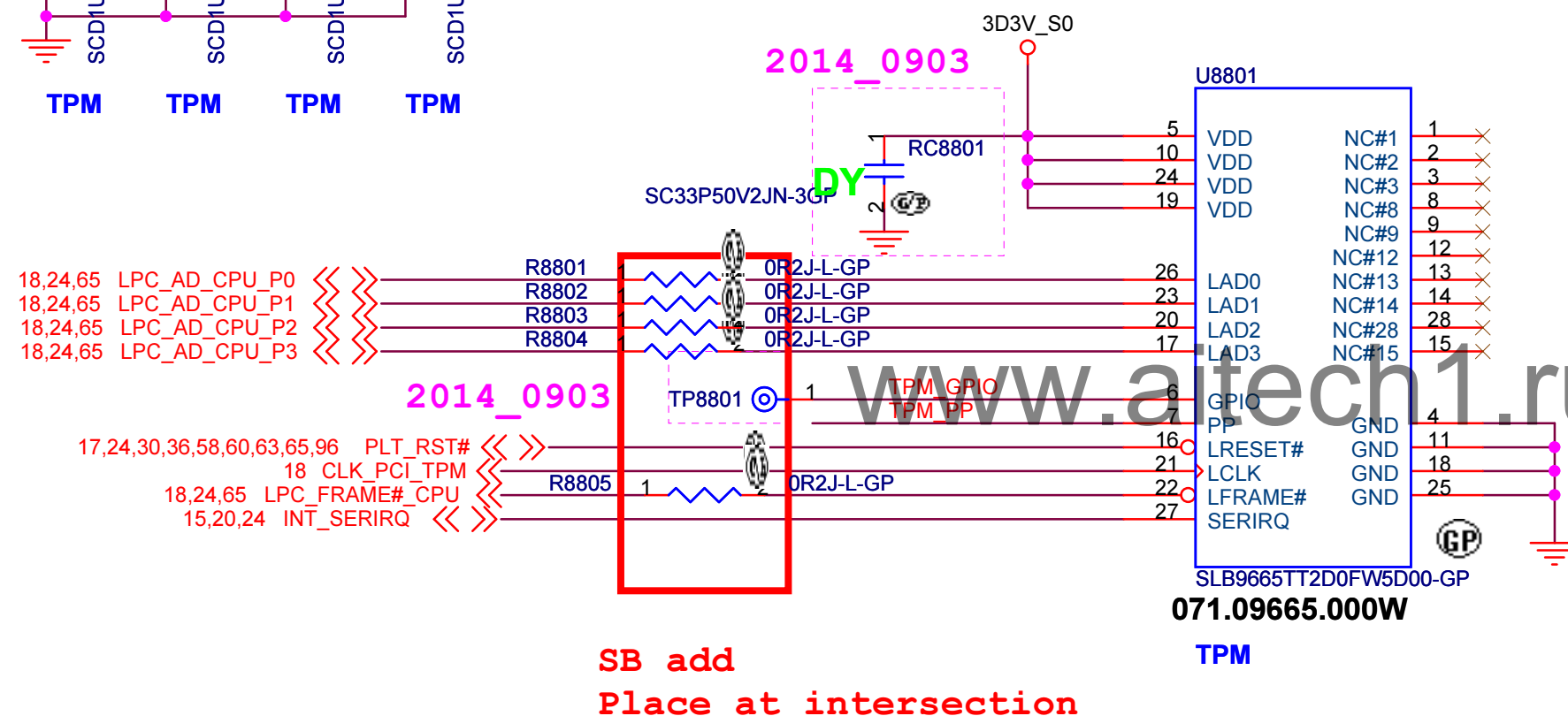
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Sheet 88 of 102

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Size A4	Document Number	Rev
Fauchon-BDW 13"		SA
Date:	Saturday, September 13, 2014	Sheet 89 of 102

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Title Switchable GFX eDP			
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Date: Saturday, September 13, 2014		Sheet 92	of 102

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Title Bottom Docking			
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Title Inter LAN WG1217LM		
Size A3	Document Number Fauchon-BDW 13"	Rev SA
Date: Saturday, September 13, 2014	Sheet 94 of	102

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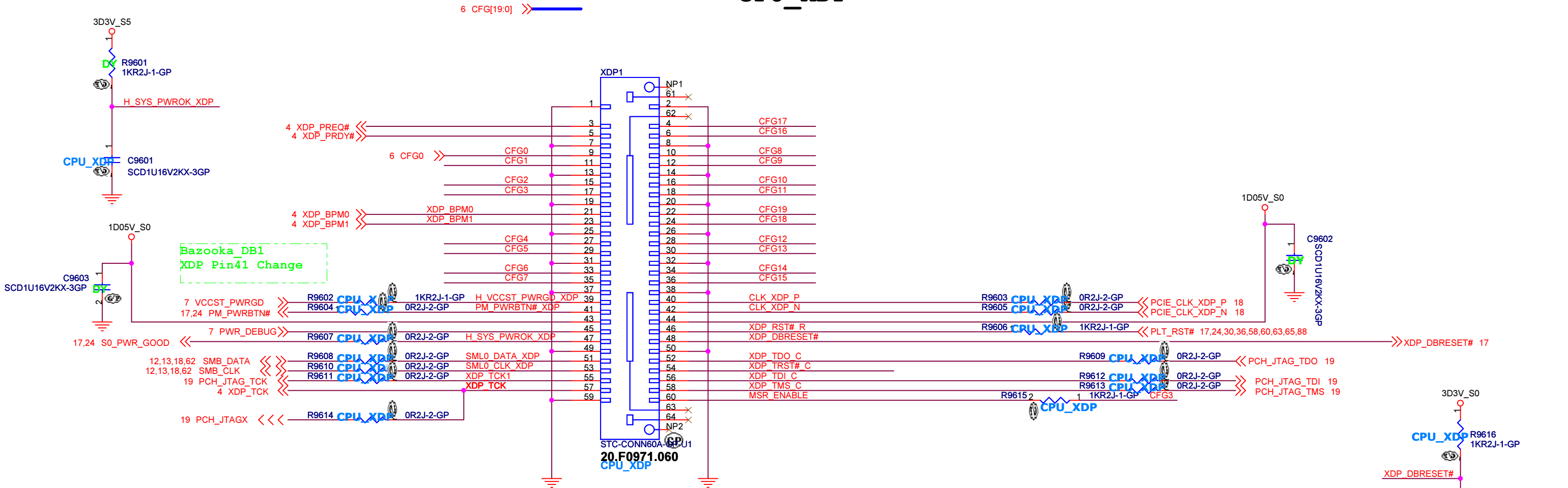
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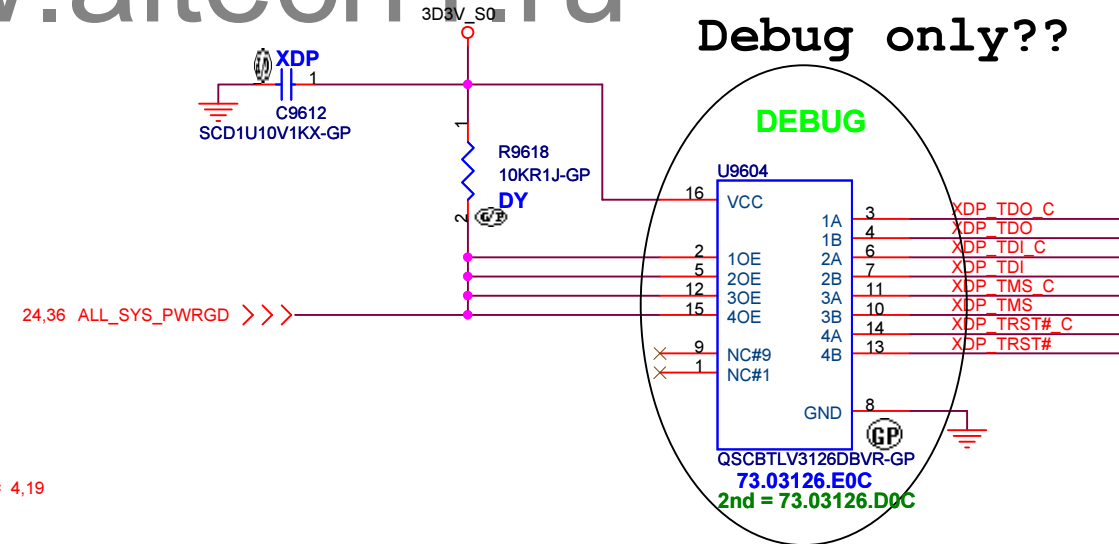
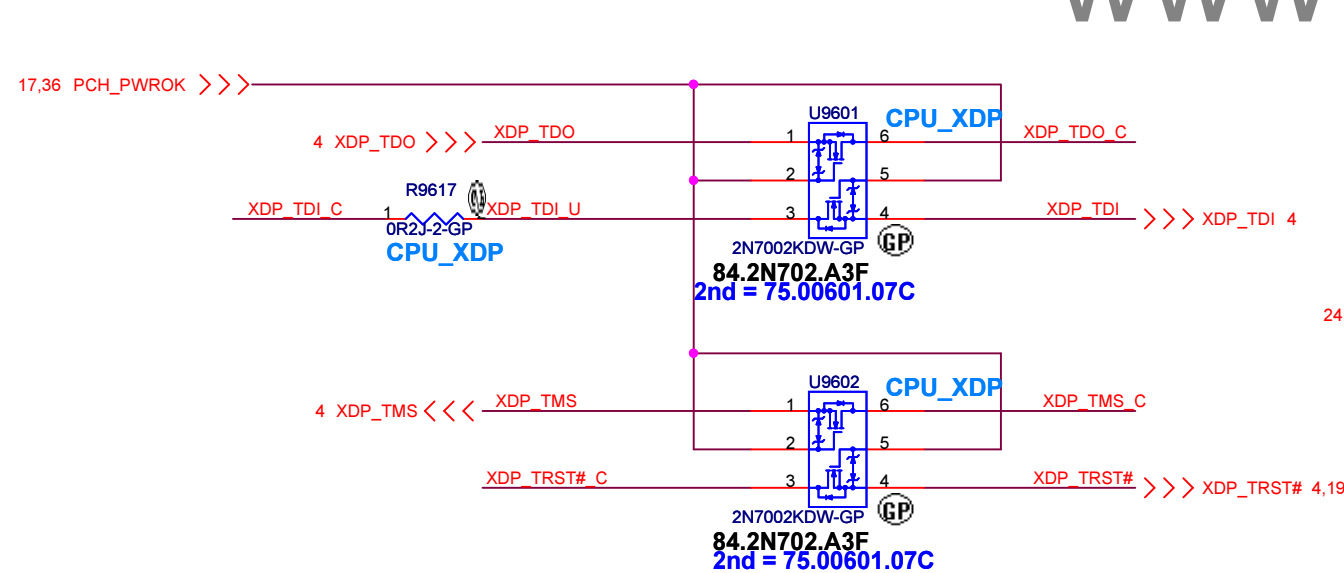
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Size A	Document Number Fauchon-BDW 13"		Rev SA
Date:	Saturday, September 13, 2014		Sheet 95 of 102

CPU_XDP



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Pin	XDP Signal Name	Target Signal	I/O	Device	Pin	XDP Signal Name	Target Signal	I/O	Device
1	OBSFN_A0	Open	I/O		2	OBSFN_A1	Open	I/O	
3	GND	GND	NA		4	OBSDATA_A[0]	Open	I/O	
5	OBSDATA_A[1]	Open	I/O		6	GND	GND	NA	
7	OBSDATA_A[2]	Open	I/O		8	OBSDATA_A[3]	Open	I/O	
9	GND	GND	NA		10	HOOK0 ¹	RSMRST#	I	System
11	HOOK1	BP_PWRGD_RST# ¹	O	System	12	HOOK2	Open	NA	
13	HOOK3	Open	NA		14	HOOK4 ¹	1.05V core	NA	
15	HOOK5	Open	NA		16	VCCOBS_AB	3.3V SUS	I	System
17	HOOK6	RSMRST# ¹	O	System	18	HOOK7	DBR# ¹	O	System
19	GND	GND	NA		20	TDO	JTAG_TDO	I	PCH
21	TRSTn	Open	NA		22	TDI	JTAG_TDI	O	PCH
23	TMS	JTAG_TMS	O	PCH	24	TCK1	Open	NA	
25	GND	GND	NA		26	TCK0	JTAG_TCK	O	PCH

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PCH_XDP			
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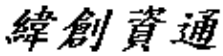
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Sheet 97 of 102

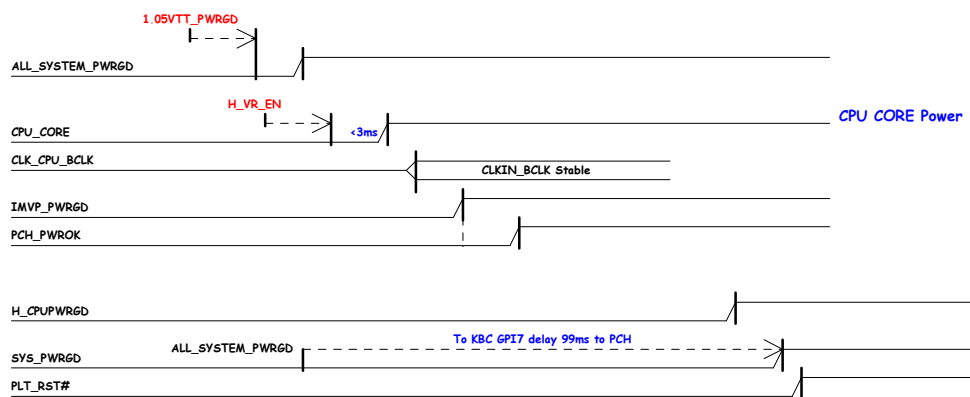
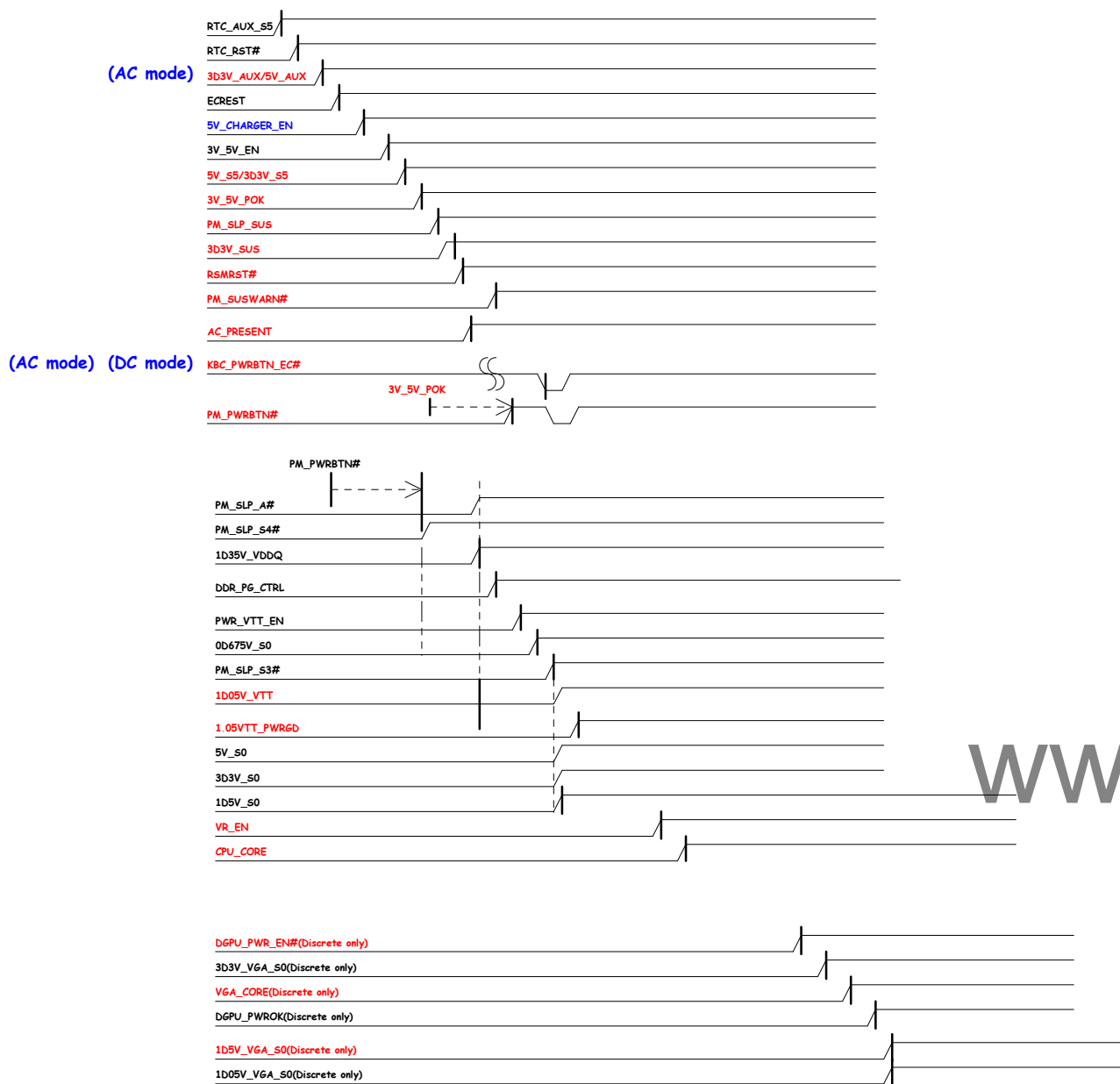
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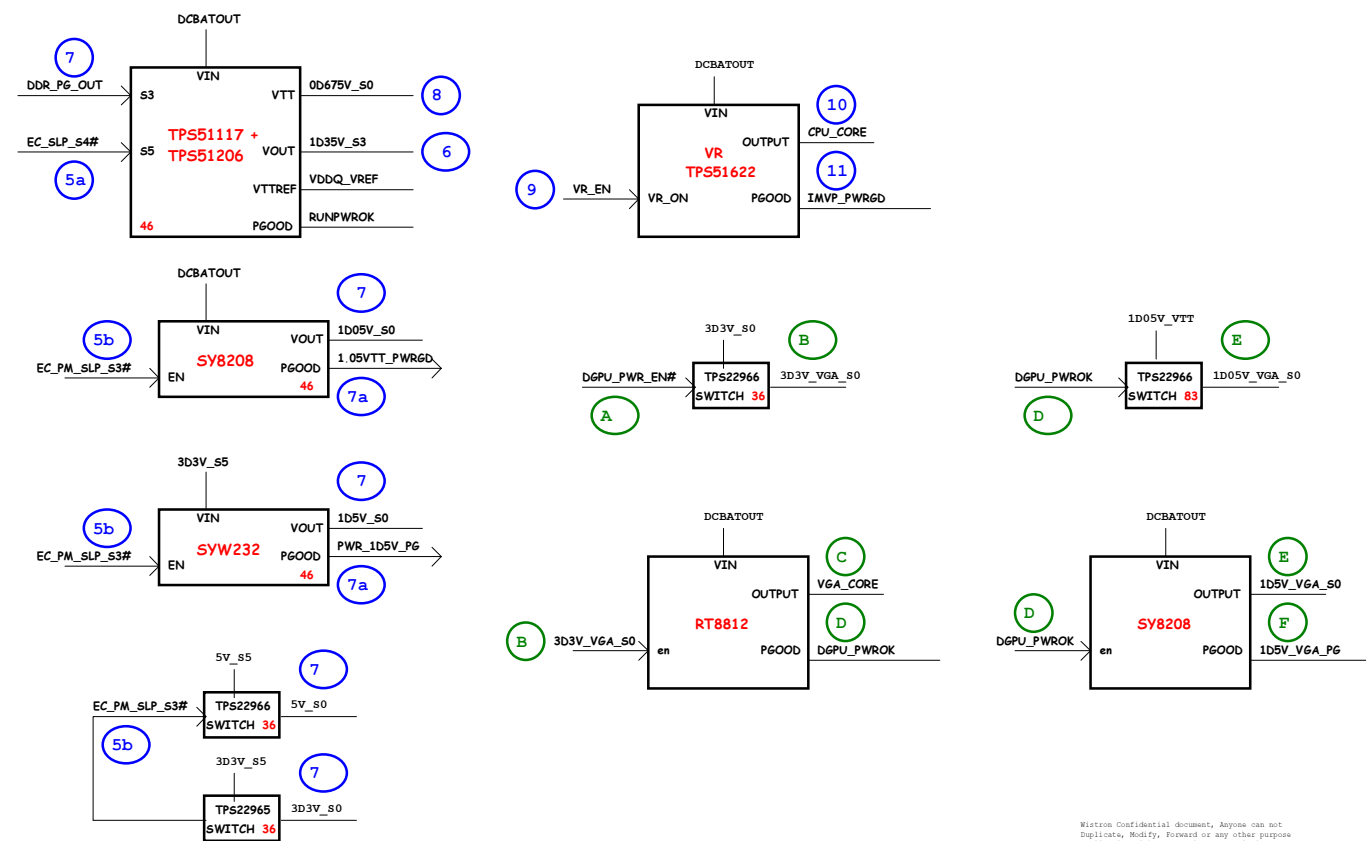
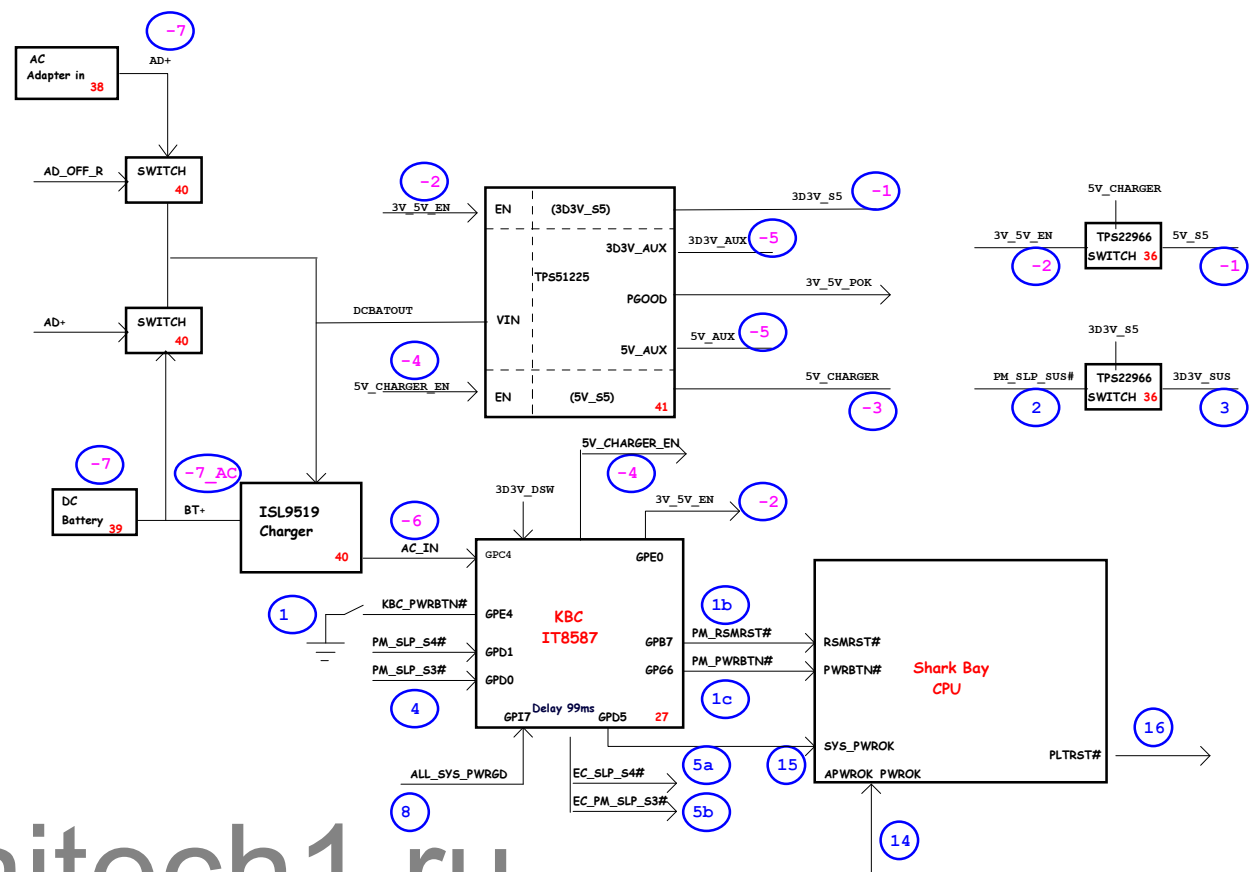
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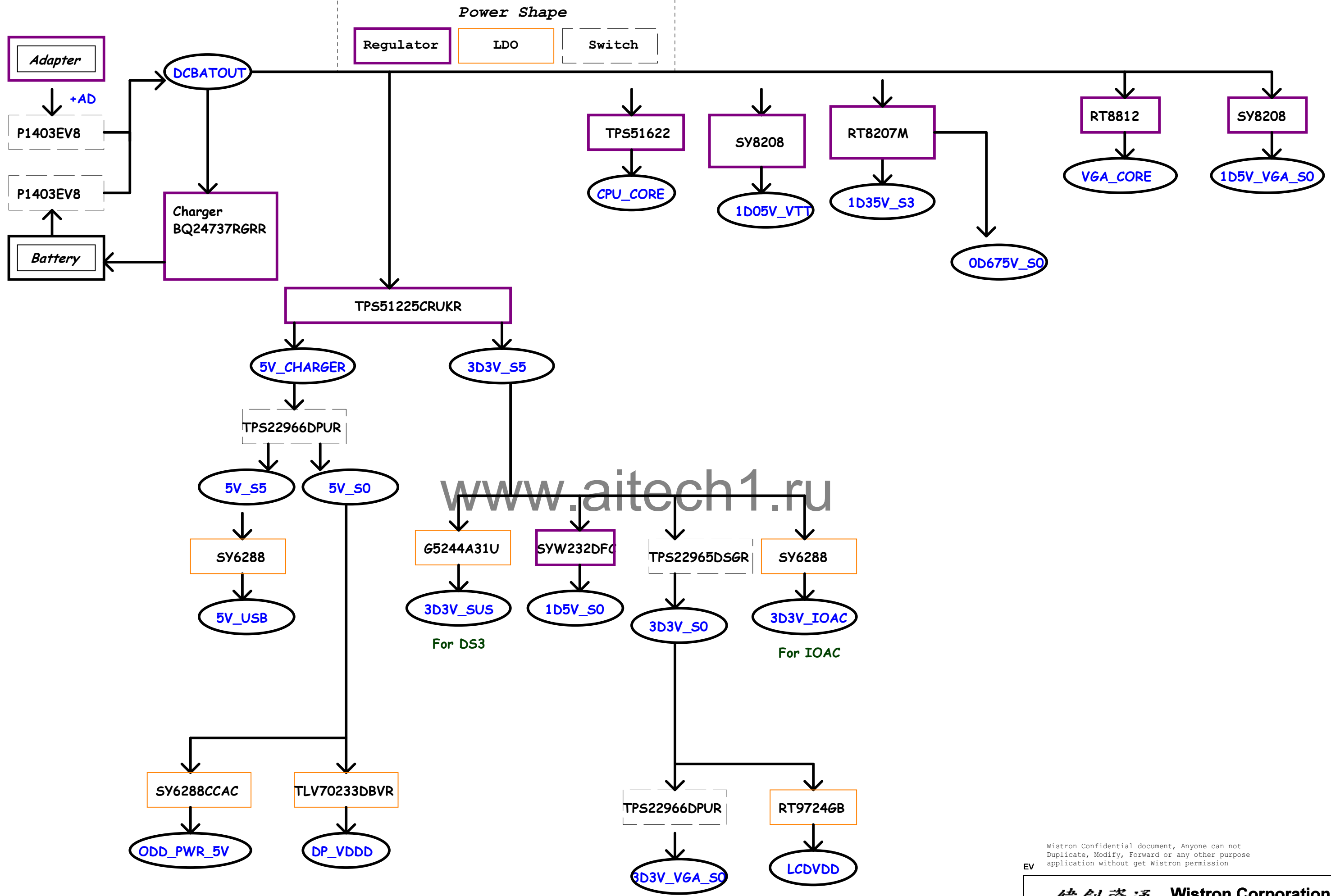
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Change History			
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Date:	Saturday, September 13, 2014		Sheet 98 of 102

Intel-Power Up Sequence

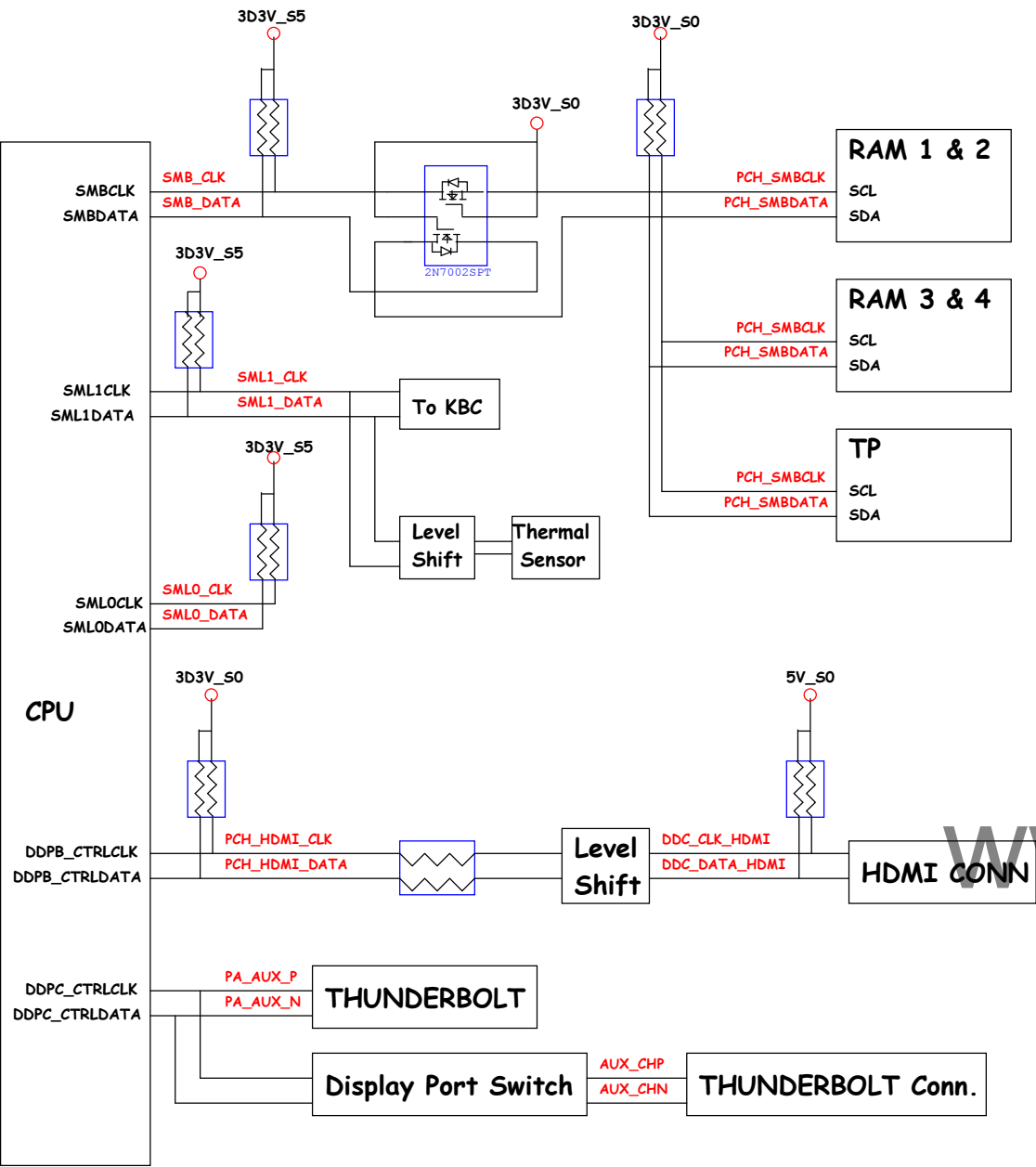


SHARK BAY POWER UP SEQUENCE DIAGRAM

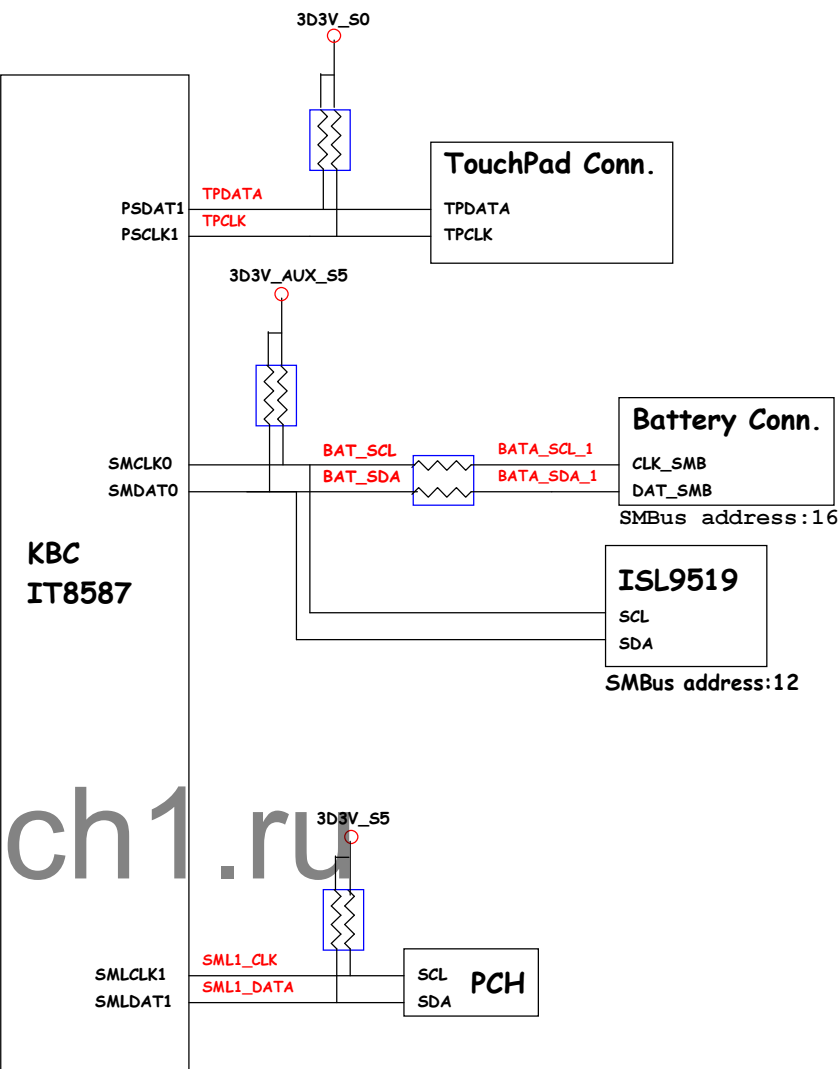




PCH SMBus Block Diagram



KBC SMBus Block Diagram



1



3

4